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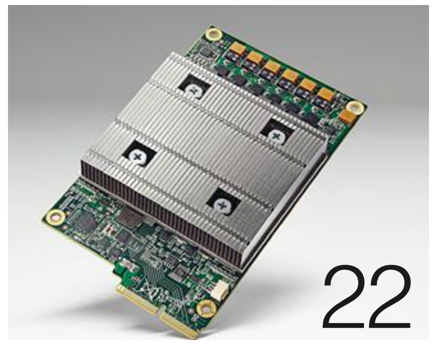
IN THIS ISSUE

FEATURES

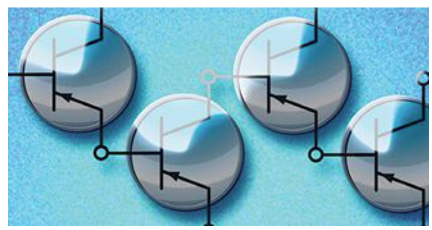
14



22

IDEAS FOR DESIGN

26



30

COLUMNS & DEPARTMENTS

33

EDITORIAL MISSION:
To provide the most current, accurate, and in-depth technical coverage of the key emerging technologies that engineers need to design tomorrow's products today.

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The Difference Between Ransomware and Malware

The number of systems being attacked using ransomware is on the rise. Technology Editor Bill Wong lays out the differences between ransomware and malware.

http://www.electronicdesign.com/industrial-automation/what-s-difference-between-ransomware-and-malware

Using Solar Power in the Industrial IoT

Solar energy harvesting can successfully power indoor applications. The key is to keep certain design considerations in mind and not to pick the battery as an afterthought.

http://www.electronicdesign.com/analog/tips-using-solar-power-your-industrial-iot-application

What Happens When Your Hardware is Insecure?

Sometimes your hardware can come back to haunt you. Case in point: Intel's Active Management Technology (AMT) has been plagued by a major bug for the past seven years.

http://www.electronicdesign.com/industrial-automation/what-happens-when-your-hardware-insecure

Welcome to Light Bulb Hell!

In his latest blog, Tech Contributor Lou Frenzel asks, "How many engineers does it take to change a light bulb?" The answer is "one," but maybe the question should be changed to: How many engineers does it take to choose a replacement light bulb? Today, it actually requires an engineer's knowledge.

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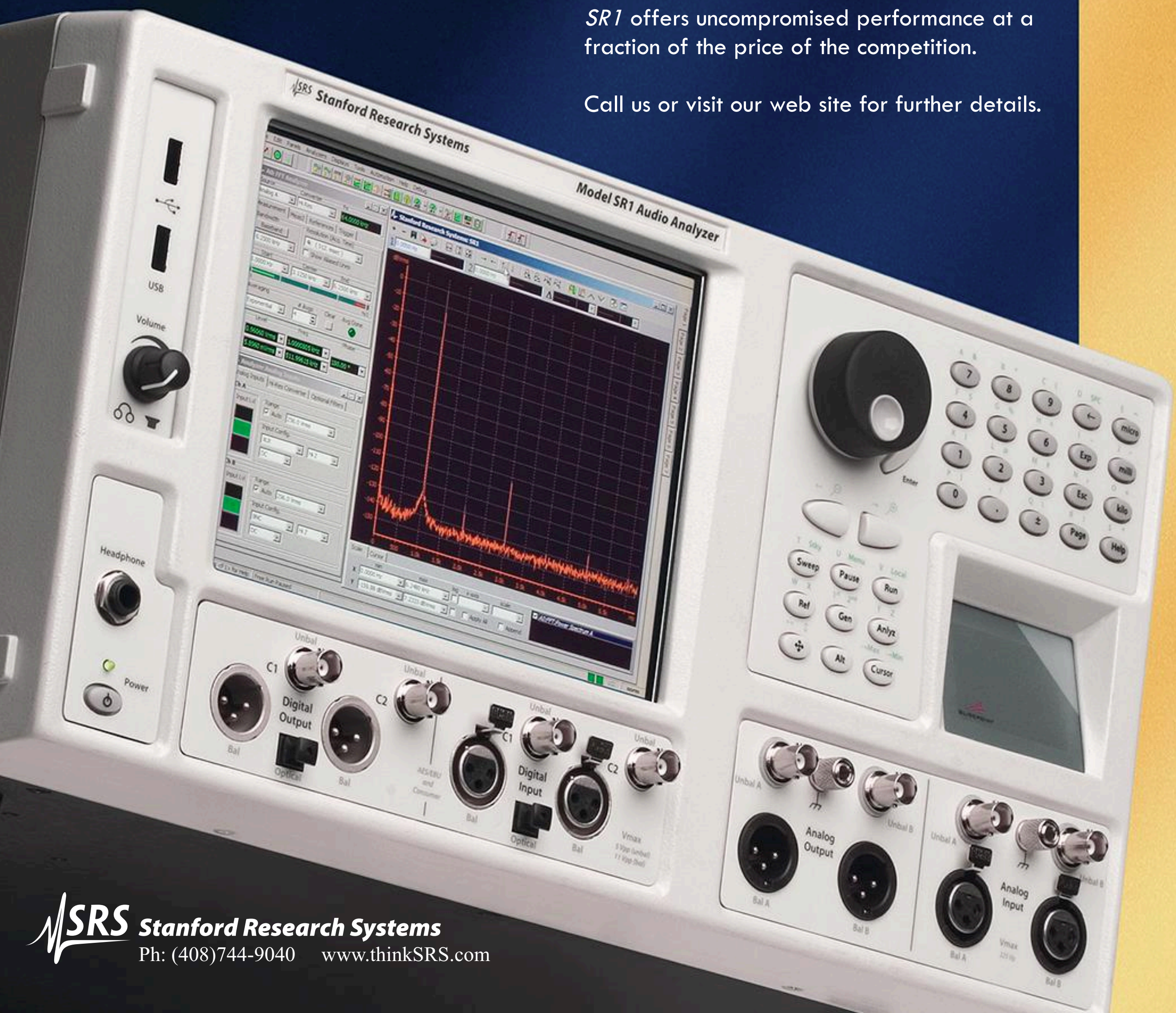

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Trump and H-1B Visas: What's to Come?

The visa program again comes under scrutiny, but it's not clear whether the recent executive order will have any impact in the foreseeable future.

Almost 20 years ago, I remember reading a column from *Electronic Design*'s then editor-in-chief talking about the controversy surrounding H-1B visas and their potential impact on EEs in the United States. As the saying goes, "The more things change, the more they stay the same," as I now sit writing this column for you.

Since the late 1990s, the controversy surrounding H-1B has at times gone quiet, but never completely died. In the engineering world, the fact is that importing talent has allowed many companies to stay competitive by hiring highly skilled and specialized engineers who were not available in the United States or not in the needed numbers. The other side of the argument points to a chicken-and-egg scenario: By not hiring U.S. engineers because they lacked certain skills or knowledge, we failed to pressure our schools and universities to "raise the bar," so to speak, thus creating a door that had to be continuously propped open. We're now in a moment in history where our current president has made unemployed workers a core focus, which has put H-1B again under fire.

To be clear, there are many fine websites and publications covering the political realm of this nation and others—and many not so fine. But our job is to cover the technology, trends, and developments in electronics engineering from our own independent—but technology- and engineering-focused—standpoint. In particular, my goal with this column is to provide an overview of what the president's intentions and plans seem to be with H-1B Visas and what impact they may have.

For anyone who doesn't know, an H-1B is a three-year visa that specifically targets workers in science, engineering, and information technology (IT). It requires the hiring company to have a need for specialized expertise and knowledge, which ideally should limit them from hiring an outside resource just to pay a lower wage. Yet it can be hard to prove that, as noted in an article from Business Insider: "Companies are required under federal regulations to declare that the H-1B workers they employ are not displacing American workers, but a loophole exempts them from that rule if the guest workers they employ are paid at least $60,000 per year. Since American tech workers usually earn higher salaries than $60,000, companies are able to hire foreign workers at lower salaries than American ones, and need not prove they are not undercutting American labor."

Issues like that loophole will not be resolved any time soon, as the presidential order is only calling for fact-finding at this stage. "In order to promote the proper functioning of the H-1B visa program, the Secretary of State, the Attorney General, the Secretary of Labor, and the Secretary of Homeland Security shall, as soon as practicable, suggest reforms to help ensure that H-1B visas are awarded to the most-skilled or highest-paid petition beneficiaries," states the "Presidential Executive Order on Buy American and Hire American."

Looking at the scope of the project, the vast number of visas that are awarded, and the different industries involved, this process will certainly be lengthy and complicated. As a result, it should have no near-term impact on Silicon Valley and high-tech companies in other parts of the country, which largely rely on outsourced engineering and technology expertise. The key is to revamp the program with enough oversight to end abuse of the salary loophole while spurring innovation and the employment of tech workers in America. Our ability to innovate must be safeguarded—but not at the expense of our workers.

Feel free to send comments to nancy.friedrich@penton.com. ed

News

NVIDIA'S LATEST CHIP
Aims 5,000 Cores at Deep Learning

Nvidia unveiled a graphics chip with more than five thousand processing cores that significantly hasten deep learning jobs in data centers. The design underlines the chip maker's belief that artificial intelligence is central to its future.

Jensen Huang, Nvidia's chief executive, announced the new product at the company's annual GPU Technology Conference in San Jose. The Tesla V100 is capable of training software on large amounts of data, applying what it has learned on new information or transferring that task to conventional computer chips.

The processor contains 21.1 billion transistors measuring only 12 nanometers, making it roughly 50% faster than Nvidia's previous graphics architecture called Pascal for traditional computing jobs. The processor's die is massive, measuring 815 square millimeters or slightly smaller than an Apple watch face.

"It is at the limit of photolithography, meaning you can't make a chip any bigger than this because the transistors would fall on the ground," said Huang, wearing his usual black leather jacket, during the opening keynote. "Just the fact that this could be manufactured is an incredible feat."

The announcement shows how seriously Nvidia is targeting customers in the market for deep learning. The chip maker poured around $3 billion into developing the Volta architecture at the heart of the V100, which contains specialized tensor cores to run mathematical operations in deep neural networks.

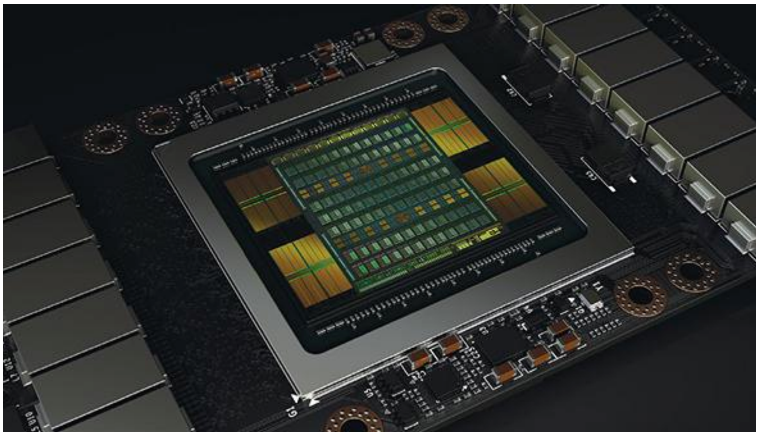
The parallel processor contains 640 such cores, which together can perform 120 trillion operations per second on deep learning workloads. It stands out not for rendering graphics but for teaching autonomous cars to drive within highway lanes or simulating what could happen if two galaxies collided.

Huang said that the new architecture would train deep learning software 12 times faster than Pascal, allowing models to be created in days rather than weeks. The cores are also six times faster at inferencing or solving new problems based on how software models are trained in data centers.

The Tesla V100 contains a new generation of HBM2 memory from Samsung as well as a novel memory controller to improve memory bandwidth 50% over Pascal. It uses Nvidia's proprietary interconnect to transfer data to computer processors at 300 gigabytes per second.

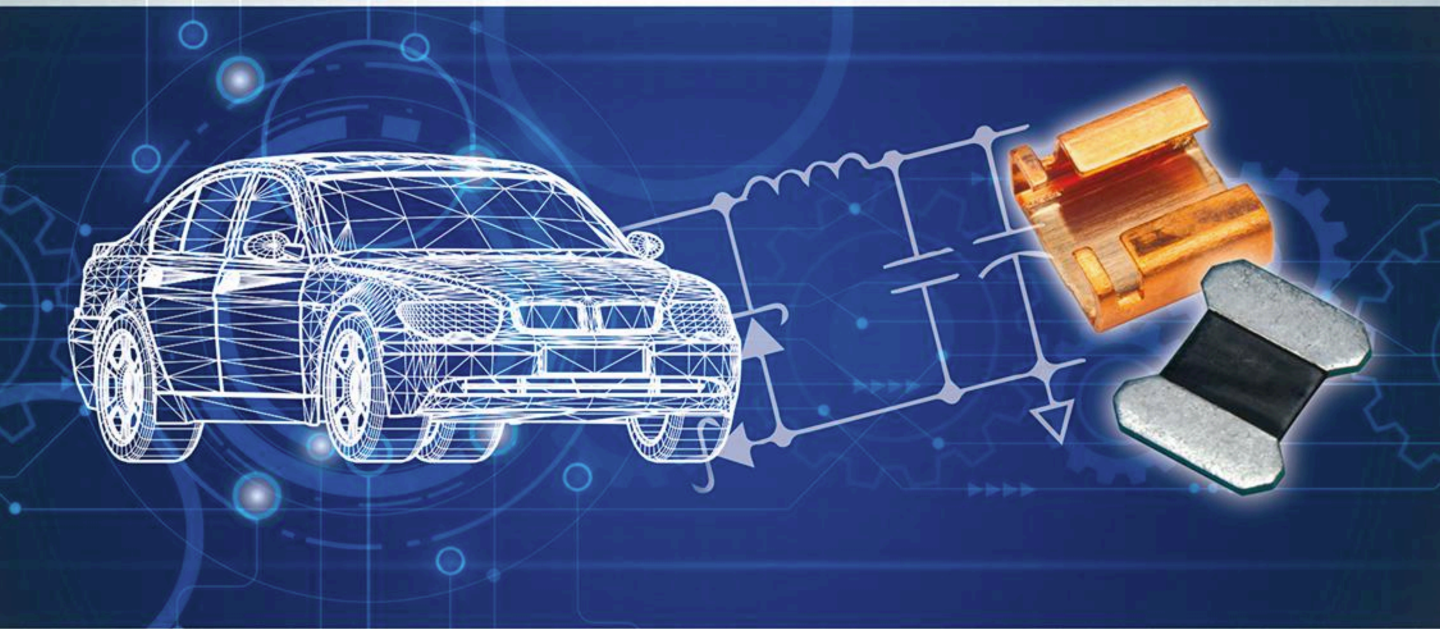
The advances amount to the clearest statement yet that artificial intelligence is the future for Nvidia, which burnished its brand in video game graphics. For years, the company has tuned its chips to handle the workloads of cloud companies like Google, Microsoft, and Amazon. Huang introduced Nvidia's own cloud computing platform this week.

Last year, Nvidia started an accelerator program called Inception that offers hardware and programming tools for start-ups in fields like medical diagnostics and predictive maintenance. Thirteen of the 15 companies funded by Nvidia's venture capital unit are involved in deep learning or autonomous driving, a field where Nvidia has supplied hardware to Audi, Mercedes, and Toyota.



The Tesla V100 contains 21.1 billion transistors measuring only 12 nanometers, making it roughly 50% faster than Nvidia's previous graphics architecture called Pascal for traditional computing jobs.

From
Concept to Reality



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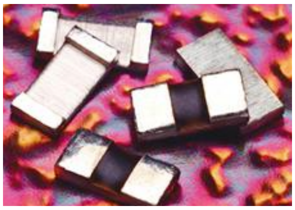

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The shift might be existential for Nvidia, but it is far from Intel's crisis of faith. Though its chips are still indispensable for data centers, the world's largest chip maker has been forced to admit that new generations of chips have failed to deliver the advances that once came from doubling the number of transistors etched onto silicon chips every two years.

For handling exhaustive tasks like voice recognition, chip makers are shifting toward specialized hardware. Two years ago, Intel acquired Altera for $16.7 billion and its vast knowledge of FPGA chips, which exhibit the same parallelism that lets graphics chips divide programs run the parts simultaneously.

Intel sells FPGAs, which can be reprogrammed on the fly, in its Go autonomous driving system as well as its Deep Learning Inference Accelerators for data centers. The chips are used as accelerators in data centers at Baidu and Microsoft, which has also built custom FPGAs for its machine learning work.

Last year, Intel spent almost $400 million on Nervana Systems, whose chief Naveen Rao—now vice president of Intel's artificial intelligence unit—had started devising custom chips to train deep learning software faster than graphics chips. Nervana argued that the chips are inefficient because they are not built for anything but graphics.

The pendulum in the semiconductor industry is swinging toward customized chips, now that internet companies are tailoring chips for machine learning. Last year, Sundar Pichai, Google's chief executive, announced that the search engine giant's had built the tensor processing unit for accelerating inferencing tasks in its data centers.

Pichai claimed that the TPU is three processor generations ahead of traditional computer and graphics chips, escaping some of the gravity of Moore's Law. The chip has been used to enhance Google's search engine and the artificial intelligence program that last year mastered the devilishly complex board game of Go.

Last month, Google unsealed the performance of its tensor processing unit, which it claims is 15 to 30 times faster than GPUs and CPUs on inferencing tasks and 30 to 80 times more energy efficient per trillion operations. Nvidia contends that Google was measuring its TPUs against older graphics chips, which are still the fastest for training software.

With the rise of custom silicon, Nvidia is increasingly finding itself in competitive cross-hairs. Trying to break into machine learning chips are a number of start-ups, including stealthy companies like Groq, which was co-founded by Jonathan Ross, a former Google engineer that helped invent the tensor processing unit.

But the Volta architecture is a powerful statement of Nvidia's head start in accelerated computing. It is not clear how badly Nvidia has been hurt by customization efforts at Google and others, but its data center business reaped $409 million in the first quarter of this year, an increase of 186% from a year earlier.

Nvidia's bet on graphics accelerators are paying dividends. The company reported first-quarter revenue of $1.94 billion, up from $1.3 billion a year earlier. Its profits soared to $507 million, up from $208 million in last year's first quarter. Nvidia's stock price jumped almost 20% during Huang's keynote, an attendee pointed out on Twitter.

"It is the reason of our existence, recognizing that we need to find a life after Moore's Law," Huang said. ■

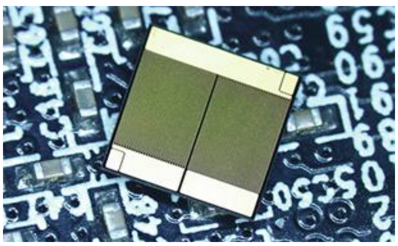
SQUEEZING 600 VOLTS Into a Voltage Regulator

RESEARCHERS BUILT what they claim is the first half-bridge circuit in a single 600-volt chip. The voltage regulator could go a long way in the development of more efficient and smaller on-board chargers in electric vehicles.

The device, unveiled by the Fraunhofer Institute for Applied Solid State Physics, is a vital component of power converters, which are used universally to control the flow of power into tablets, washing machines, and anything else with a power cord. In electric cars, the voltage regulator could help shorten battery charging time.

The device's hallmark, the researchers say, is that all its infinitesimal parts share the same slab of gallium nitride, also known as GaN, an advanced semiconductor that inherently handles higher voltages and temperatures than traditional silicon. That enables vastly faster switching speeds, which only hit around 30 MHz in many current devices.

The layout of the monolithic chip includes two GaN transistors grown on silicon substrates, as well as a pair of diodes that suppress sudden voltage spikes from the power supply. The layout also helps to minimize negative effects like line impedance, improving the electrical switching characteristics. ■



All of the new chip's parts share the same slab of GaN, which inherently handles higher voltages and temperatures than traditional silicon.

SourceToday

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4	Future Electronics Inc.****	$5 billion (EST)
5	TTI Inc.	$1.99 billion
6	Digi-Key Electronics	$1.8 billion
7	Electrocomponents plc/Allied Electronics, Inc.******	$1.778 billion
8	Premier Farnell*****	$1.382 billion
9	Mouser Electronics	$1.034 billion
10	Rutronik Elektronische Bauelemente GmbH*******	$921 million
11	N.F. Smith & Associates	$810 million
12	DAC/Heilind	$790 million
13	Fusion Worldwide	$405 million
14	Sager Electronics	$258 million
15	PEI-Genesis	$206 million
16	Master Electronics	$203 million
17	America II Electronics	$200 million
18	Advanced MP Technology	$180 million
19	Bisco Industries Inc.	$148 million
20	Powell Electronics	$127 million
21	Electro Enterprises Inc.	$109.7 million
22	Flame Enterprises	$95.5 million
23	Steven Engineering Inc.	$93 million
24	RFMW Ltd.	$91.7 million
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41	House of Batteries	$22.1 million
42	Area51-ESG, Inc.	$20.2 million
43	PUI (Projections Unlimited)	$18.3 million
44	Cumberland Electronics Strategic Supply Solutions	$18 million
45	Kensington Electronics	$17.5 million
46	CTrends	$17.2 million
47	Gopher Electronics Company	$16.5 million
48	Advantage Electric Supply	$15 million
49	Marine Air Supply	$15 million
50	4 Star Electronics Inc.	$10.2 million

*Avnet 1: On September 19, 2016, Avnet announced it had entered into an agreement to sell its TS business to Tech Data Corp. Figures on global or company-wide results include TS figures (revenue, products, and employees.) The transaction closed in February 2017

** Avnet 2: Americas: All Avnet figures given here are for the Americas region, which includes North America, Argentina, Brazil and Puerto Rico.

*** Avnet 3: On October 17, 2016, Avnet finalized its acquisition of Premier Farnell. Revenue figures are included for 11 of the 13 weeks in the December quarter.

****SourceToday estimate of Future Electronics global revenue

*****SourceToday estimate of Premier Farnell full fiscal year February 1, 2016 - January, 2017

******Estimate of Electrocomponents FYH22016 + FYH12017 (October 2015-September 2016)

*******Rutronik's reported revenue in euros (Applied average exchange rate of 12/30/2016) EUR = 1.0566

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LOU FRENZEL | Contributing Editor

Long-Range IoT on the Road to Success

Newer wireless technologies known as LWPANs offer a lower-cost option for Internet of Things applications that demand longer-range paths.

Most engineers consider the Internet of Things (IoT) as a collection of short-range wireless technologies that connect devices to the internet for some useful purpose. And most current IoT applications seem to fall into that category. However, that mindset is changing.

Many wireless standards are limited by their range, which is problematic for a number of useful applications that require much longer paths. To overcome that hurdle, a collection of newer longer-range wireless technologies have emerged. Called low-power wide-area networks (LPWANs), these links fill the gap between traditional short-range technologies and the more costly M2M alternatives *(see table)*.

WHAT IS LONG RANGE?

There's no formal definition for long range, but today's most popular technologies have essentially set its parameters in place. One prominent maximum range is 10-30 meters. Bluetooth, ZigBee, and 802.15.4-based technologies use this figure as a guideline, but longer ranges are also possible under

COMPARING LPWAN TECHNOLOGIES					
Technology	Frequency	Data rate (max)	Range	Power	Cost
2G/3G	Cellular bands	~10 Mb/s	Several km	High	High
Ingenu	2.4 GHz	624 kb/s	Many km	Low	Medium
LoRa	915 MHz	<50 kb/s	15 km	Low	Low
LTE-M	Cellular bands	1 Mb/s	Several km	Medium	High
NB-IoT	Cellular bands	250 kb/s	Several km	Medium	High
SigFox	<1 GHz	100-1000 b/s	Several km	Low	Medium
Symphony	915 MHz	<50 kb/s	Up to 10 km	Low	Medium
Weightless	<1 GHz	0.1-24 Mb/s	Several km	Low	Low
Wi-Fi (11af/ah)	<1 GHz	0.1-1 Mb/s	Several km	Medium	Low

favorable conditions. Wi-Fi is said to have a maximum usable range of 100 meters, but it's typically less than that. Even shorter ranges from standards like IrDA, NFC and RFID max out at a foot or so.

All of these standards are useful, as evidenced by the IoT successes so far. Nonetheless, some industrial and public utility applications simply need more range to be viable.

For this article, I define long range as anything greater than a few hundred meters up to 30 to 50 miles. LPWAN vendor LinkLabs defines long range as up to 10 km. Applications requiring such range involve the monitoring and/or control of some equipment or system. Examples include the smart grid and utility water or gas metering. Other longer-range uses include city lighting control and agriculture monitoring. Most of the available short-range technologies cannot reliably deliver the ranges necessary for these applications.

ACHIEVING LONGER RANGE

The range of a radio signal is determined by a number of factors: frequency of operation, transmitter power, antenna gains, receiver sensitivity, antenna height, physical obstructions (e.g., buildings and trees), data rate, and noise and interference. While all are important, perhaps the one that carries the most weight is frequency. The basic physics of wireless says that lower frequencies travel farther than higher frequencies. Path distance is directly proportional to wavelength (λ), where wavelength is:

$$\lambda = 300/f_{MHz}$$

As the frequency shrinks, the range lengthens. That holds true for signals with line-of-sight (LOS) propagation. LOS infers that the transmitting antenna can "see" the receiving antenna. Signals above about 50 MHz have this characteristic, but it's more pronounced at UHF, microwave, and millimeter-wave frequencies.

Frequencies below 1 GHz do exhibit some non-LOS characteristics (meaning they can penetrate walls and trees to a degree), making them desirable when direct LOS isn't possible. That's one reason why cellular frequencies in the 800- to 1000-MHz range are so coveted. And that's why much of the newly reassigned 600- and 700-MHz bands are being sold to cellular operators.

You can also see this range vs. frequency phenomenon by looking at the radio path-loss equation.

$$\text{dB path loss} = 37\text{ dB} + 20\log(f) + 20\log(d)$$

Distance (d) is in miles and frequency (f) is in MHz.

Now consider the location of the most popular IoT technologies. Yep, the unlicensed 2.4-GHz band. Newer Wi-Fi versions like 11ac and 11ax use 5 GHz. Wi-Fi, Bluetooth, ZigBee, and 802.15.4 derivatives like Thread, ISA100a, and others use the 2.4 GHz unlicensed band. The power level is also restricted—no wonder range is limited. In some applications, mesh networking can help extend range, but that's for special cases that require many nodes.

Other key factors influencing range are data rate and noise. Higher speeds tend to limit range, with noise playing a major role in the bit error rate (BER). Lower data rates consume less bandwidth, and a smaller bandwidth limits the noise, creating a more reliable connection. Using higher levels of modulation (e.g. QAM) boosts speed. However, it's more susceptible to noise, making the link less robust. Range automatically goes up as data rate drops, since it's generally more immune to noise.

Most LPWAN technologies work with a total path loss in the 130- to 180-db range, far greater than the typical path loss in the 90-db range of traditional wireless technologies. This requires a receiver sensitivity of –130 dBm or better for a good connection. Such sensitivity levels are possible with the narrower bandwidths and lower data rates of LPWAN products.

While longer range is the key feature of LPWANs, lower data rate and low power consumption are also core features. How low is low data rate? One definition says that it's less than 5 kb/s with fewer than 200 bytes per message. It can be as low as several hundred bits per second or as high as 100 kb/s. Even higher rates are possible at reduced range.

Another important factor is very low power consumption. Most applications assume battery-powered nodes in this context. To make the LPWAN viable, battery life is crucial—it must be years, even five to 10 years by some standards.

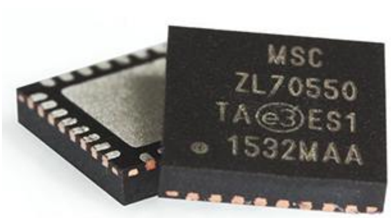
Most of the newer long-range technologies take these qualities into account and can deliver the extended links required by many applications. In no particular order, let's take a look at what's available:

ISM BAND

Most of the standards discussed here utilize the unlicensed industrial-scientific-medical (ISM) bands set aside by the FCC in Part 15 of the Code of Federal Regulations (CFR) 47. The most widely used ISM band is the 2.4 - to 2.483-GHz band, which is the province of Wi-Fi, Bluetooth, 802.15.4 radios, and many others. The 902-928 MHz band is the next most-used, with 915 MHz being a sweet spot. Other popular ISM frequencies are 315 MHz for garage-door openers and remote-keyless-entry (RKE) applications and 433 MHz for remote temperature monitoring. In the UK and Europe, 169 MHz and 868 MHz are popular.

Many simple wireless applications don't require complex network connections, security, or other custom features, which makes it possible to design simple proprietary protocols. Many vendors of ISM-band transceivers offer standard protocol support and development systems that can be used to develop a protocol for a specific application.

For example, Microsemi developed the ZL70550 ISM band transceiver *(Fig. 1)* for LPWAN products. It can operate on any frequency in the 779- to 965-MHz range making it useful in the U.S. and most other countries. Transmit power is 0 dBm and receiver sensitivity is -106 dBm. Data rates of 50, 100, or 200 kb/s can be selected. The chip includes the Z-Star protocol, a MAC layer that eliminates any need for external processor involvement in packet processing.



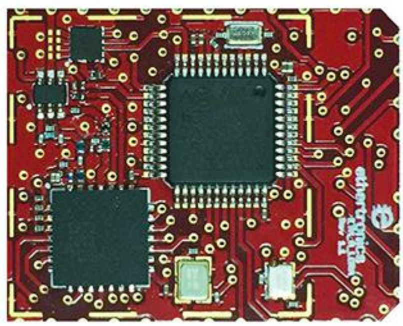
1. Microsemi's ZL70550 transceiver IC, targeted at ISM band LPWAN applications, comes in a 32-pin QFN package measuring 5 × 5 mm.

LoRa

LoRa, which means long range, is a relatively new wireless technology from Semtech Corp. that's designed to extend the range of LPWAN for IoT and M2M applications. LoRa uses the 902- to 928-MHz unlicensed band in the U.S. and the 868-MHz band in Europe. Typical operating frequencies are 915 MHz for the U.S., 868 MHz for Europe. and 433 MHz for Asia.

The LoRa physical layer (PHY) uses a unique form of FM chirp spread spectrum along with forward error correction (FEC). This spread-spectrum modulation permits multiple radios to use the same band if each radio has a different chirp and data rate. Data rates extend from a low of 290b/s to 50 kb/s. A key feature is very low power consumption. Typical range is 2 to 5 km and up to 15 km is possible (depending on the location and antenna characteristics)—far greater than most of the other short-range technologies.

A unique LoRa product is Ethertronics' ETH-M-LORA-AX *(Fig. 2)* module that incorporates Semtech's SX1272 LoRa transceiver and the Ethertronics EC686 antenna impedance tuner chipset. It provides active beamsteering to produce multiple radiation patterns, thus optimizing the link connection and ensuring link reliability.



2. The ETH-M-LORA-AX module, developed by Ethertronics, implements LoRa and provides active antenna tuning and steering to maximize link reliability.

CELLULAR

Cellular networks for IoT applications are generally known as machine-to-machine (M2M) networks. Multiple vendors offer cell-phone modules to embed into other products, and most major cellular carriers provide M2M connection services over standard licensed spectrum.

Though 2G technology like GSM/GPRS/EDGE was popular, some carriers are already phasing out 2G operation. However, most carriers still support 3G technologies like WCDMA and cdma2000 with data rates up to several megabits per second. Range is simply the distance to a cell site, and can be up to several kilometers. Cellular connectivity is clearly an option, although the equipment and service are more expensive than most of the other LPWAN systems described here. The main benefit of cellular is that it gives the subscriber a global network.

Virtually all cellular carriers use LTE or Long Term Evolution, the current 4G technology. It's widely implemented in the U.S. and around the world. With its megabit data rates, LTE is overkill for most IoT/M2M applications.

New versions of LTE, designated Cat 0 and Cat 1, are reduced-function versions of LTE designed for low power and low speed to match the needs of IoT/M2M use cases. These applications use the existing cellular network in licensed spectrum rather than short-range wireless and the

3. Housed in a package measuring a mere 6.5 × 8.5 mm, Sequans Communications' Monarch module is a complete LTE-M radio designed for IoT and M2M applications.

4. The SARA-N200 module is u-blox's NB-IoT module for the 900-MHz cellular band. It comes in a 16- × 26- mm package.

internet. Cat 0 and Cat 1 utilize the existing LTE bandwidths, with orthogonal frequency-division multiple-access (OFDMA) modulation. This is a long-range solution capable of kilometers of distance. The most popular LTE standards are called LTE-M and NB-IoT.

LTE-M for machine uses a 1.4-MHz channel and standard LTE resource blocks with 15-kHz subcarrier spacing. The uplink employs OFDMA and up to 16QAM to achieve a peak data rate up to 1 Mb/s. The downlink uses SC-FDMA for a peak rate of 1 Mb/s. Its low-power modes make it suitable for many IoT/M2M applications. One popular LTE-M module, the Monarch, comes by way of Sequans Communications *(Fig. 3).*

Narrowband IoT, or NB-IoT, uses one resource block of twelve 15-kHz LTE subcarriers. It's 180 kHz wide in a 200-kHz channel. Data rates peak at 250-kb/s uplink and 170-kb/s downlink with a modulation of OFDMA downlink and SC-FDMA uplink. This further simplified standard enables very low power consumption in devices.

NB-IoT is deployed in any LTE network as a software overlay. A resource block of NB-IoT fits nicely inside a standard LTE channel or within a guard band. *Figure 4* shows a typical NB-IoT module for the 900-MHz cellular band. This u-blox model has peak data rates of 62.5-kb/s uplink and 27.2-kb/s downlink.

SIGFOX

Sigfox is a wireless technology as well as a network service. SigFox is a French company offering its wireless technology as well as a local LPWAN for longer-range IoT or M2M applications. It operates in the 868- and 915-MHz ISM bands but consumes very little bandwidth or power.

SigFox radios leverage a technique called ultra-narrowband (UNB) modulation in the form of binary phase-shift keying (BPSK), which only transmits short messages at low data rates occasionally. Data rates in a 200-kHz channel can be from 100 to 1000 b/s. Messages can be up to 12 bytes long and a node is able to send up to 140 messages per day. Because of the narrow bandwidth, short messages, and 162-dB link budget, long range up to 30 to 50 km is possible.

INGENU

Ingenu is both a technology and a network. Like Sigfox, Ingenu builds networks in specific areas of coverage and provides hardware and software to provision the application. Unlike most of the other LPWAN vendors, Ingenu uses the 2.4-GHz unlicensed band. That would limit range, but the technology deploys coding techniques that provide very high processing gain resulting in super sensitive receivers that help extend the range.

Ingenu's technology is called random-phase multiple access (RPMA). It uses direct-sequence spread spectrum (DSSS) and differential BPSK modulation, and achieves a peak data rate of 634 kb/s. Code-division multiple access (CDMA) is used to support multiple users in common channel. In addition to supplying its own network, Ingenu claims a coverage area considerably larger than most other LPWAN methods, and can accommodate many more users per access point (gateway).

SYMPHONY

Symphony is LinkLabs' LPWAN offering. It uses the LoRa PHY, but features a custom media-access-control (MAC)

If higher performance is needed with two-way communication, Weightless-P could be the ticket. It uses a combination of FDMA and TDMA to manage access to multiple 12.5-kHz-wide channels. Data rates can range from a low of 200 b/s to 100 kb/s using GMSK and offset QPSK modulation.

software layer. While the PHY delivers the robust link, it's the MAC that ensures the network created can manage the connections required of the application. Features of the Symphony MAC include that it's an open standard, repeaters are used to assist coverage where needed, it has an adaptive data rate, and offers scalable capacity. Other characteristics are MAC-layer packetization, 100% acknowledgement of messages, uplink power control, and low downlink latency.

WEIGHTLESS

Weightless is a family of open wireless-technology standards targeting IoT applications. Three versions address different segments of the LPWAN marketplace. The simplest version is Weightless-N for low cost applications, such as simplex or one-way uses like sensor monitoring. Modulation for this technology, which operates in the sub-1-Gbit license-free ISM, is differential BPSK using a frequency-hopping technique to minimize interference. One key feature is its 128-bit AES encryption with full authentication. With low data rates and narrow channels, a range up to 5 km is possible. Low power consumption permits a battery life of up to 10 years.

If higher performance is needed with two-way communication, Weightless-P could be the ticket. It uses a combination of FDMA and TDMA to manage access to multiple 12.5-kHz-wide channels. Data rates can range from a low of 200 b/s to 100 kb/s using Gaussian minimum shift keying (GMSK) and offset quadrature-phase-shift-keying (QPSK) modulation. Typical maximum range is about 2 km. AES 128/256 encryption and authentication are used for security.

Finally, Weightless-W is designed to operate in the TV white spaces. White spaces are those 6-MHz-wide channels previously used by TV stations in the 470- to 790-MHz band. It's possible to achieve data rates from 1 kb/s to 10 Mb/s, depending on the link budget. A range of 5 km or more is possible in non-line of sight situations. Use of the TV white spaces requires the base stations to reference a master database of TV bands and wireless microphone frequencies and choose an unused band to avoid interference. Weightless is a royalty-free IP that helps to minimize cost.

WI-FI

Standard Wi-Fi versions like 802.11a/b/g/n/ac/ax can be used for IoT, but it's usually not the optimal choice. Power consumption is generally high and its available data rate goes far beyond what's needed for most applications. However, two versions of Wi-Fi are a good fit for long-range uses.

White-Fi, or 802.11af, is designed to utilize the TV white spaces or unused TV channels from 54 to 698 MHz. These 6-MHz channels are ideal for supporting long-range and non-line-of-sight transmission. The standard employs cognitive radio technology to ensure no interference to local TV signals. The base-station queries a database to see what channels are available locally for data transmission. The modulation is OFDM using BPSK, QPSK, or QAM. Maximum data rate per 6-MHz channel is about 24 Mb/s, and ranges up to tens of miles are expected at the lower VHF TV frequencies.

Another IoT-friendly version of Wi-Fi is called HaLow. The standard, designated 802.11ah, uses the 902- to 928-MHz license-free band in the U.S. and similar bands just below 1 GHz in other countries. This is good news, because low power can be used over these lower frequencies, thus enabling battery-operated equipment. While most Wi-Fi gear has a maximum range of 100 meters under ideal conditions, HaLow can reach up to a kilometer with the right antenna.

Modulation for 11ah is OFDM using 24 subcarriers in a 1-MHz channel and 52 subcarriers in the larger bandwidths. Modulation can be BPSK, QPSK, or QAM providing for a wide range of data rates. Rates of 100 kb/s to several megabits per second will do in most cases. Its real goal was low power. The Wi-Fi Alliance says it will implement an 802.11ah testing and certification program by 2018.

Both the 11af and 11ah standards are complete. However, there's no appropriate silicon, so there's been only a handful of adoptions. These are good alternative solutions for long-range circumstances. ed

WILLIAM WONG | Technical Editor

CPUs, GPUs, and Now AI Chips

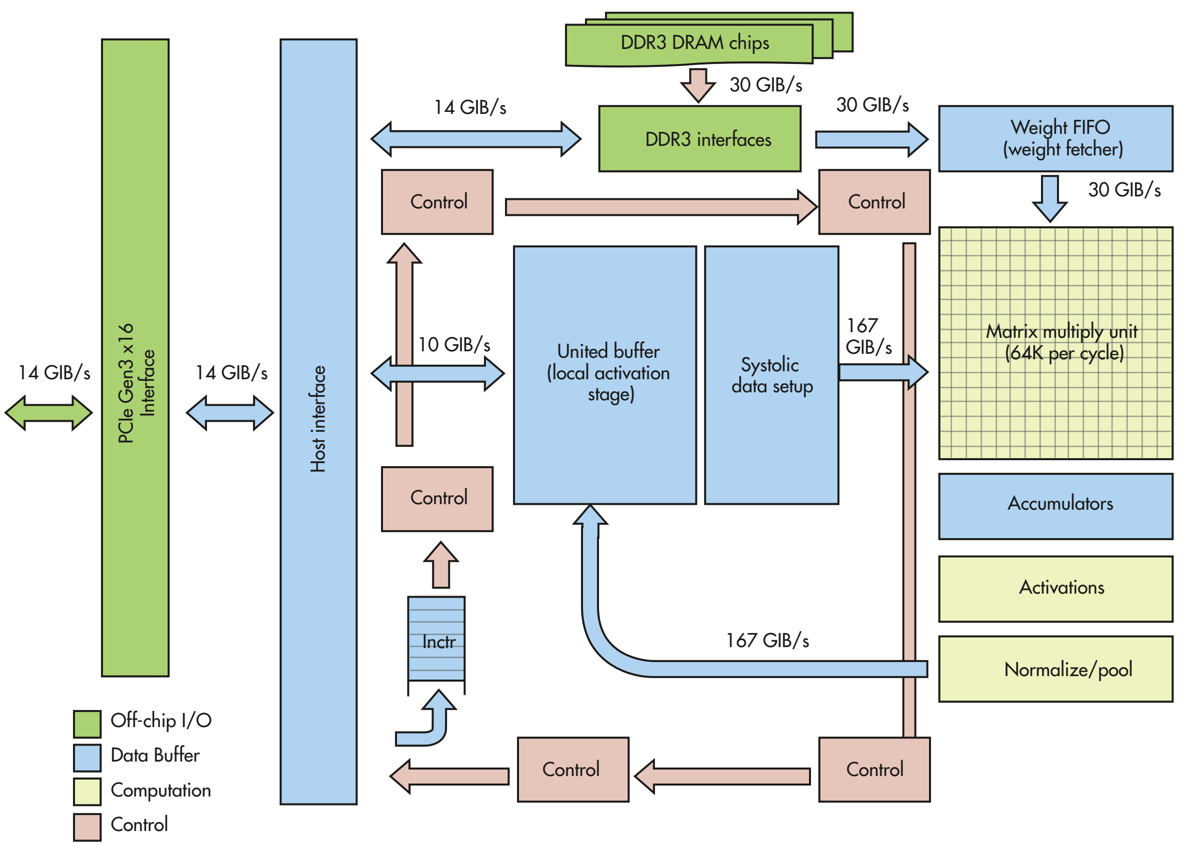
First it was CPUs. Next came GPUs. What's next? How about AI chips?

If you haven't heard about the artificial intelligence (AI) machine-learning (ML) craze that uses deep neural networks (DNN) and deep learning (DL) to tackle everything from voice recognition to making self-driving cars a reality, then you probably haven't heard about Google's new Tensor Processing Unit (TPU), Intel's Lake Crest, or Knupath's Hermosa. These are just a few of the vendors looking to deliver platforms targeting neural networks.

GOOGLE TPU

The TPU contains a large 8-bit matrix multiply unit *(Fig. 1)*. It essentially optimizes the number-crunching required by DNN; large floating-point number-crunchers need not apply.

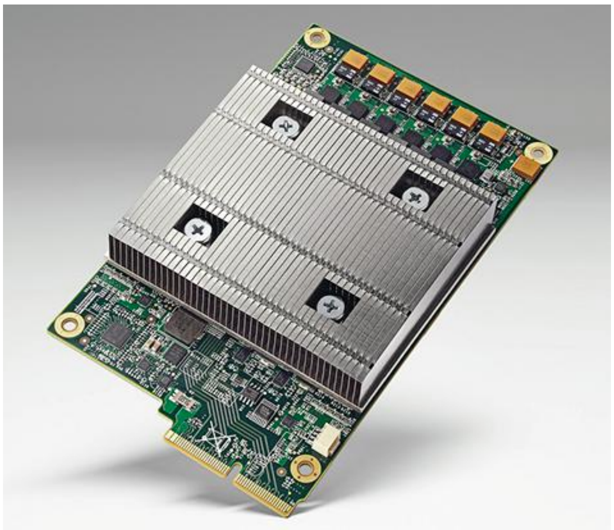
The TPU is actually a coprocessor managed by a conventional host CPU via the TPU's PCI Express interface. The TPU chip runs at only 700 MHz, but can best CPU and GPU



1. Google's TPU has a large 8-bit matrix multiply unit to help it crunch numbers for deep neural networks.

systems when it comes to DNN acceleration. Though not specifically a DNN processor, it handles the heavy lifting while consuming only 40 W of power. It has 28 Mbytes of on-chip RAM along with 4 Mbytes in the form of 32-bit accumulators used to compile the 16-bit results from the matrix multiply unit. The chip uses a 28-nm process and the die size is about 600 mm^2. The paper "In-Datacenter Performance Analysis of a Tensor Processing Unit" provides more details.

The TPU board *(Fig. 2)* can perform 92 TeraOps/s (TOPS). It is 15 to 30 times faster than CPUs and GPUs tasked with the same work, with a 30- to 80-fold improvement in TOPS/W. The software used for comparison of systems was the TensorFlow framework.



2. Google's TPU module is designed to fill arrays of slots in its cloud data centers.

One thing to keep in mind is that TPU comparisons are done with respect to its limitations. Most CPUs are 64-bit platforms and GPUs can have wider word widths. They also tend to be optimized for larger data items, although most systems have support for smaller word sizes (including 8-bit vector operations). Likewise, different neural network applications benefit from different configurations, but the smaller 8-bit integers have found wide application in many DNN applications.

The TPU is has five primary instructions:

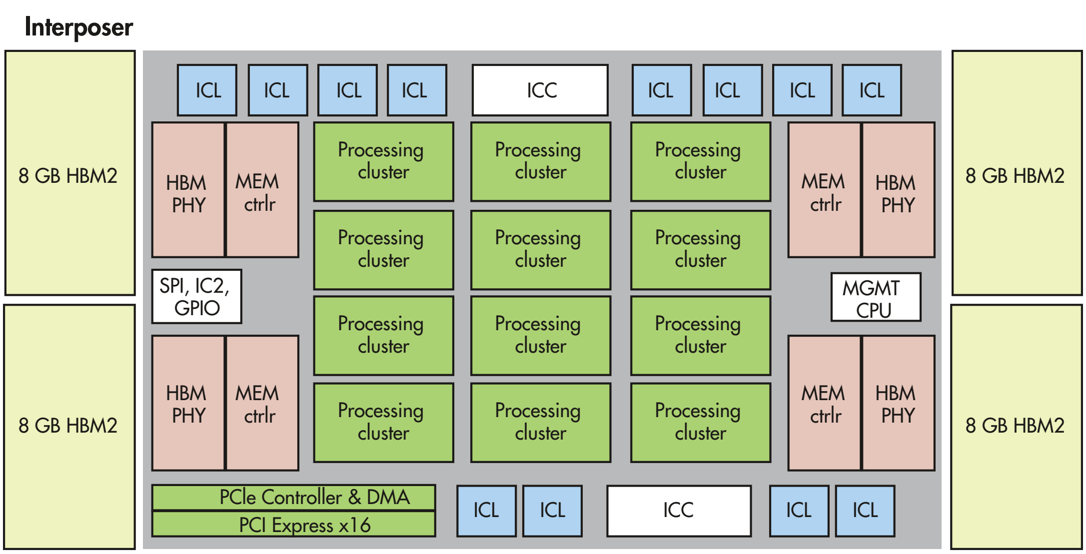
- Read_Host
- Read_Weights
- MatrixMultiply/Convolve
- Activate
- Write_Host

Weights are values within a neural network and are used by the matrix multiply unit. The activate function performs a nonlinear operation for an artificial neuron.

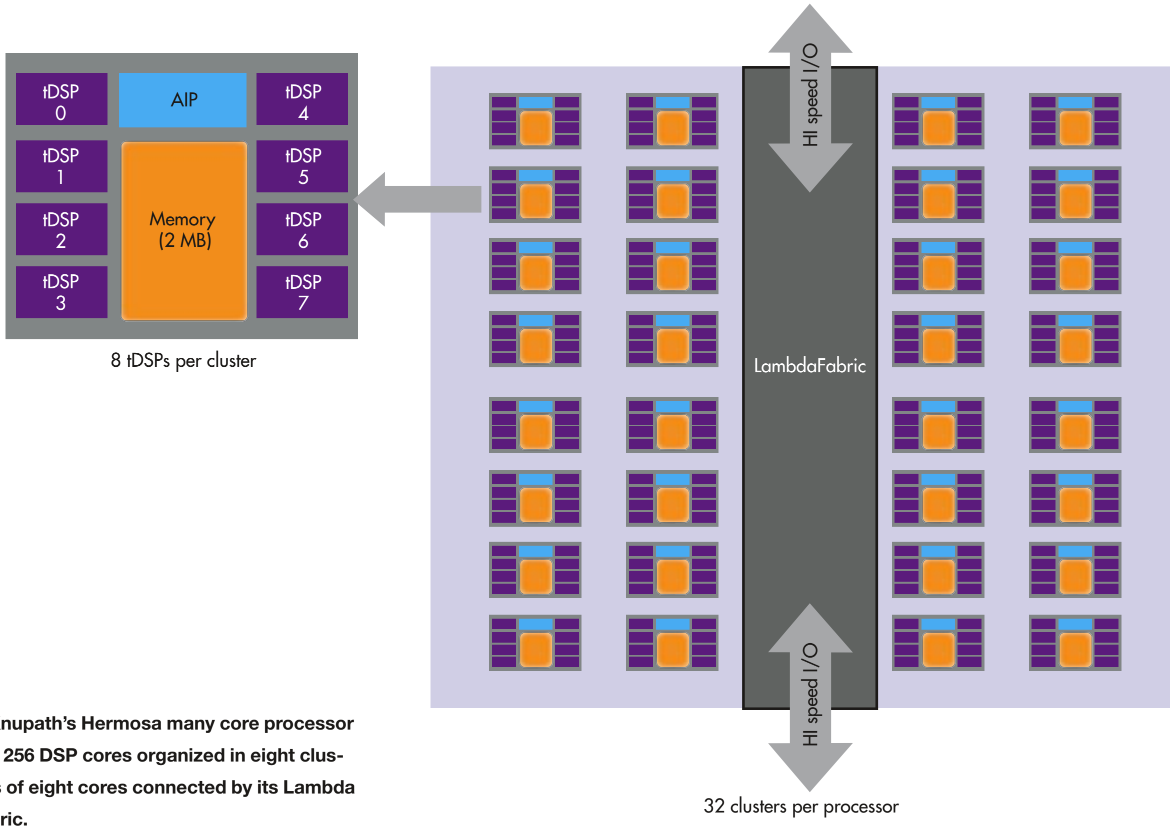
Google's TPU is expected to reduce the need for larger data centers that would otherwise need many more CPUs and GPUs to handle the AI applications addressing everything from voice recognition and analysis, to image and video processing, to providing services from search, to those little Google Home systems.

INTEL LAKE CREST

Lake Crest *(Fig. 3)* is the codename for an Intel platform designed to complement the many-core Xeon Phi *(see "Integrated Fabric is Key to Many Core Platforms" on electronicdesign.com)*. The Xeon Phi has been tasked with many AI chores, but it can be challenged by applications that Google's TPU or Intel's Lake Crest will readily handle more efficiently.



3. Intel's Lake Crest uses processing clusters optimized for AI applications.



4. Knupath's Hermosa many core processor has 256 DSP cores organized in eight clusters of eight cores connected by its Lambda Fabric.

Lake Crest technology was originally developed by Nervana, which is not part of Intel.

The new chip will employ a range of advanced features from MCM (Multi Chip Module) design to the "Flexpoint" architecture with a dozen specialized, multicore processing nodes like the TPU's matrix multiply unit. The chips will have 32 Gbytes of High Bandwidth Memory 2 (HBM2) with an aggregate bandwidth of 8 Tbytes/s attached via an interposer. HBM2 has become common in high-performance SoCs and GPUs. Lake Crest does not have any caches. Software will be used to optimize memory management.

Lake Crest is expected in the 2017 timeframe.

KNUPATH HERMOSA

Knupath's Hermosa *(Fig. 4)* has 64 DMA engines and 256 DSP cores organized in eight clusters of eight cores connected by its Lambda Fabric. The Lambda Fabric is also designed to link thousands of Hermosa processors in a low latency and high throughput mesh.

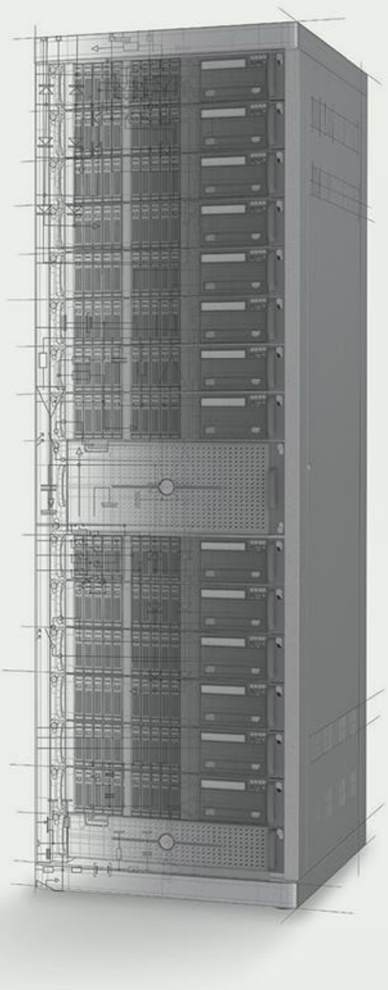
The Hermosa has an integrated L1 router with 32 ports and a 1 Tbit/s bandwidth. Links to the outside world include 16 10 Gbit/s bidirectional ports. The chip has 72 Mbytes of data RAM organized in 32 banks and 2 Mbytes of program RAM.

Although Hermosa targets AI applications, it may be more akin to the many-core Xeon Phi than the more specialized Lake Crest or TPU platforms. Hermosa only uses 34 W to deliver 384 GFLOPS of computing power, making it very interesting for a wide range of applications—not just AI ones.

GPGPUS CONTINUE TO REIGN (FOR NOW)

NVidia and AMD have a vested interest in their GPU platforms, which have been the backbone for most high-end neural network work. This could change as specialized AI chips become available. The question is how tailored these chips will be to a particular application, how available they will be, and how well they can be applied to different applications.

Right now GPU platforms like NVidia's Jetson TX2 *(see "DNN Popularity Drives NVidia's Jetson TX2" on electronicdesign.com)* are being used in everything from drones to medical devices. It is actually possible to be used in an AI accelerator in Intel's tiny Curie module, as well *(see "What Is Inside an IoT Chip?" on electronicdesign.dom)*. One size does not fit all, but AI will only continue grow in importance for computer applications. ed



MARIA GUERRA | Technology Editor

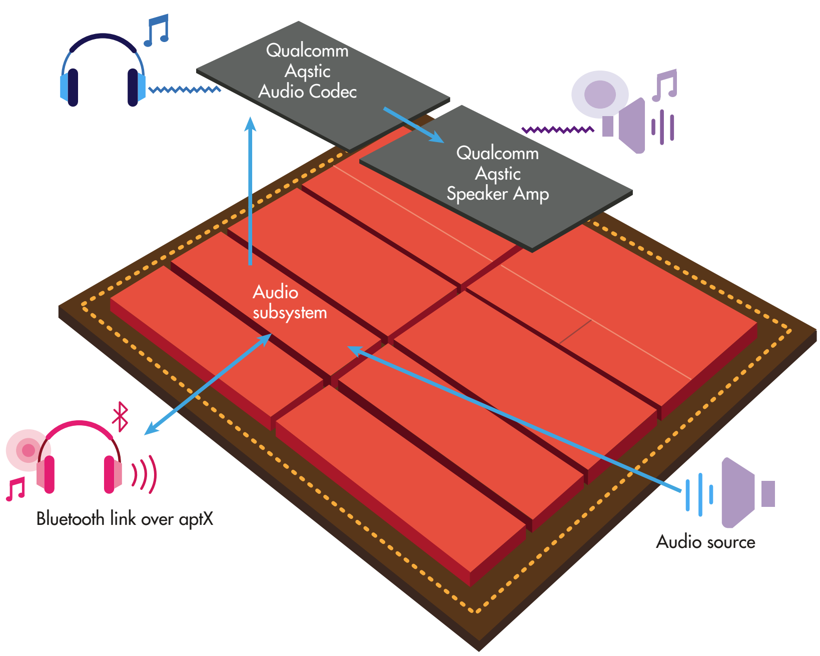
WHAT DO PHONES AND MUSIC Have in Common?

Audio data converter products are evolving based on the needs of the consumer electronics segment.

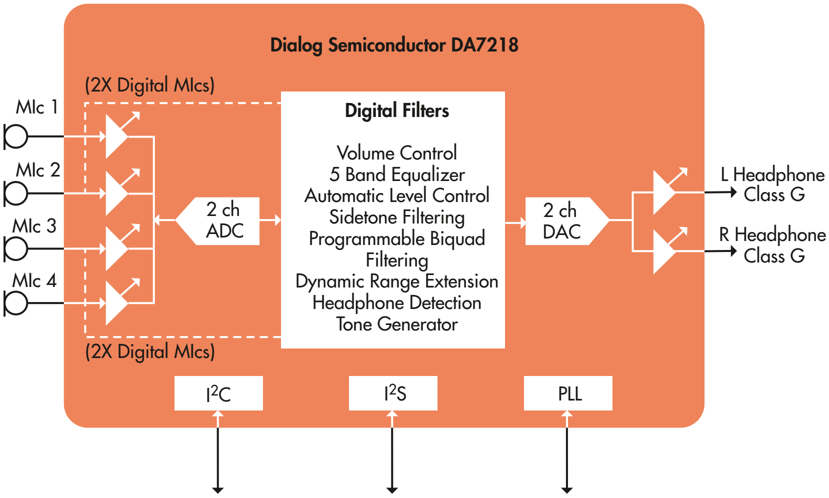
With the increasing adoption of smartphones and tablets, the demand for audio codecs also is growing. To satisfy the high standards of audiophiles, audio ICs are also evolving in terms of their level of sophistication and quality. The demand for a high-quality audio experience with smartphones is rising as mobile users use their phones not only to talk or text but to listen to music or play other multimedia content. Simply put, users want to have a better audio experience and if they are into music, they want the best possible audio experience.

This trend is pushing audio-codec designers to build audio solutions that will improve wired and wireless audio experiences while using consumer electronic such as phones, headphones, virtual reality headsets, etc. Power consumption keeps being one of the challenges at the time of decoding signals and including more functionality into programmable DSPs can be challenging but beneficial because they can adapt an audio codec to perform new functions or adapt audio codecs to be used in new applications or even comply with emerging standards.

System integration, for example, is becoming more common in the audio codec market. For example, Qualcomm Technologies recently integrated Qualcomm Aqstic technology into the Qualcomm Snapdragon 835 processor. The Qualcomm Aqstic WCD9341 audio codec *(Fig. 1)* has an integrated digital-to-analog converter (DAC) that supports up to 192-kHz/24-bit playback. As is typical, the performance of this new audio codec is



1. Snapdragon processors audio architecture is designed to optimize both wired and wireless audio *(Courtesy of Qualcomm)*



2. The DA7218 has the ability to run the ADCs at a different sample rate to the DACs *(Courtesy of Qualcomm)*

In applications such as audio accessories, wired headsets, and wired headphones, there are several options in the audio codec market. A number of high-performance, low-power audio codecs can support the always-on audio detect function now present in many consumer audio devices.

measured in terms of signal-to-noise ratio (SNR) and total harmonic distortion + N (THD + N). With an SNR at 115 db, it can also support dual oscillators. The dual-clock design supports sampling frequencies of 44.1 kHz and 48 kHz, independently.

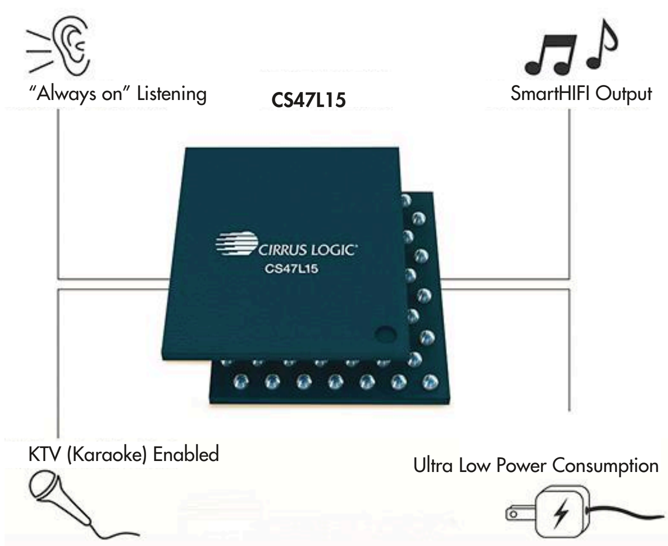
In applications such as audio accessories, wired headsets, and wired headphones, there are several options in the audio codec market. A number of high-performance, low-power audio codecs can support the always-on audio detect function now present in many consumer audio devices. Dialog Semiconductor, for instance, offers the DA7218 *(Fig. 2)*, a high-performance low-power audio codec optimized for use in portable applications or wearable devices.

In a 32-ball WLCSP with 0.5 mm pitch, the DA7218 contains stereo audio analog to digital converters (ADCs) that can run either in low-power mode for always-on applications or in high-performance mode for other applications, improving power consumption. It features voice mode filtering up to 32 kHz with a high-performance stereo-DAC-to-headphone playback path with 100 dB SNR.

Cirrus Logic (the company that supplies audio chips used in iPhones) offers the CS47L15 *(Fig. 3)*, a smart codec with low power consumption that enables OEMs to cost-effectively incorporate advanced audio features. Examples include “always on” voice activation, enhanced karaoke, and virtual stereo and protection algorithms for emerging enhanced speaker playback.

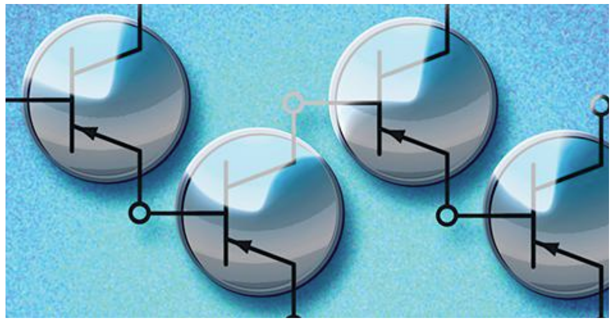
The device has an integrated multichannel 24-bit, hi-fi audio hub codec with 98-dB signal-to-noise ratio (SNR) mic input (48 kHz) and 127-dB SNR headphone playback (48 kHz). The CS47L15 provides battery life savings by maximixing the battery life in voice, music, and standby modes. The power, clocking, and output driver architectures are designed to .ow-power (25 µW). Sleep Mode is supported, with configurable wake-up events. An additional supply is required for the Class D speaker drivers (typically direct connection to 4.2-V battery).

Audio codec manufacturers are taking new challenges by enhancing the audio experience of the new multimedia trends: wireless headphones, phones, virtual reality. There is no doubt that audio codecs are elevating the audio experience for mobile users and with the data speeds benefits of the upcoming 5G network the quality of audio will only get better.



3. The CS47L15 supports SPI™ and I2C interface modes for control-register access. *(Courtesy of Qualcomm)*

MARIA GUERRA | Technical Editor

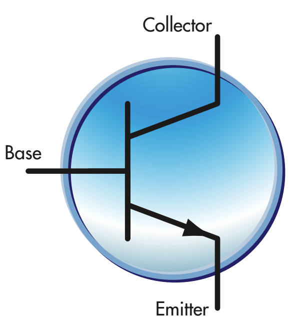


Comparing PNP and NPN

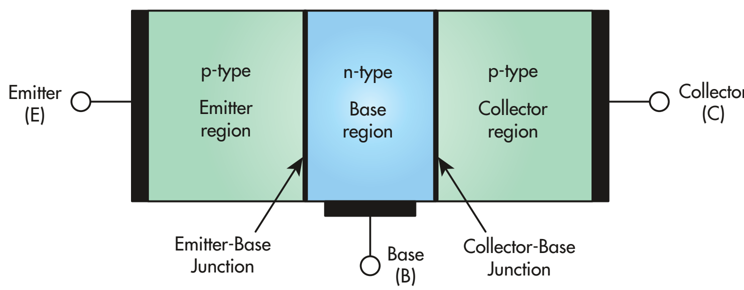
Transistors are semiconductor devices capable of amplifying signals or switching circuits. Although millions of them—in different varieties—are found in integrated circuits across every electronic device, here we focus specifically on bipolar junction transistors.

There are two main types of transistor: bipolar junction transistors (BJTs) and field effect transistors (FETs). BJTs are made of doped materials and can be configured as NPN and PNP. A transistor is an active device with three terminals, and these three terminals are known as the Emitter (E), the Base (B), and the Collector (C) *(Fig. 1)*. The Base is responsible for controlling the transistor while the Collector is the positive lead, and Emitter is the negative lead.

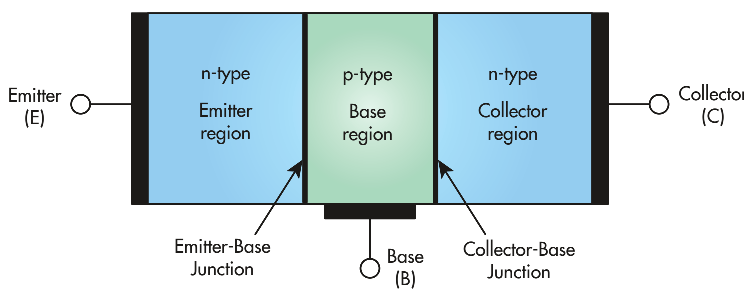
The semiconductor physics of BJTs will not be discussed here, but it is worth mentioning that a BJT is fabricated with three separately doped regions with two junctions. The PNP transistor has one N region between two P regions *(Fig. 2)* while the NPN transistor has one P region between two N regions *(Fig. 3)*. The junctions between N and P regions are similar to the junctions in diodes and they can be forward-biased or reverse-biased as well. BJTs can operate in different modes depending on the junction bias:



1. The transistor symbol indicates the three terminals. *(Courtesy of Quora)*



2. A PNP transistor has a layer of N-doped semiconductor between two layers of P-doped material. *(Courtesy of Wikibooks)*



3. A NPN transistor has a layer of P-doped semiconductor between two N-doped layers. *(Courtesy of Wikibooks)*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MEMORY PROTECTION DEVICES
DL2032
DURACELL
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MPD
MEMORY PROTECTION DEVICES

- Cutoff: BJT operates in this zone in switching operations. In cutoff, the transistor is inactive.

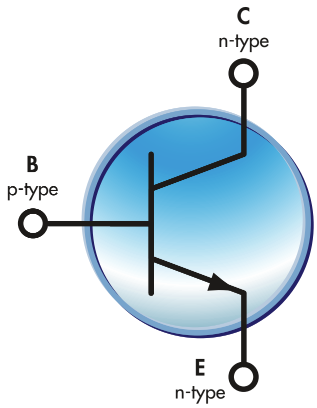
- Active: BJT operates in this zone for amplifier circuits because the transistor can act as a fairly linear amplifier.

- Saturation: BJT operates in this zone in switching operations. The transistor appears as a near short circuit between the collector and emitter terminals.

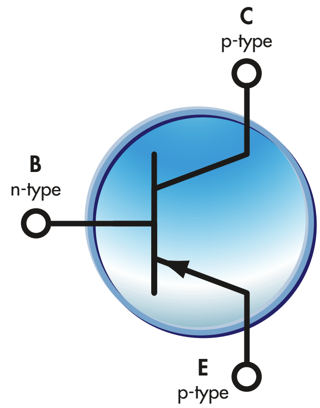
- Reverse Active: Like active mode, the current is proportional to the base current, but flows in reverse. This mode is rarely used.

In an NPN transistor, a positive voltage is given to the collector terminal to produce a current flow from the collector to the emitter. In a PNP transistor, a positive voltage is given to the emitter terminal to produce current flow from the emitter to collector. In an NPN transistor, the current flows from the collector (C) to the Emitter (E) *(Fig. 4)*. In a PNP transistor, however, the current flows from the emitter to the collector *(Fig. 5)*.

The arrow shows the direction of the current and how it is always on the emitter.



4. The NPN transistor always has an arrow pointing out.



5. The PNP transistor always has an arrow pointing in.

It is clear that the current directions and voltage polarities in PNPs and NPNs are always opposite to each other. NPN transistors require a power supply with positive polarity with respect to common terminals, but PNP transistors require a negative power supply.

PNPs and NPNs work pretty much alike, but their modes are different because of the current polarities. For example, to put an NPN into saturation mode, VB should be higher than VC and VE. Here is a summary of the operation modes depending on their voltages:

Voltage Relations	NPN	PNP
$V_E < V_B < V_C$	Active	Reverse
$V_E < V_B > V_C$	Saturation	Cutoff
$V_E > V_B < V_C$	Cutoff	Saturation
$V_E > V_B > V_C$	Reverse	Active

Here is a list of some classic general-purpose BJTs:

Part	Type
2N2222	NPN
2N2907	PNP
2N3904	NPN
2N3906	PNP

The basic principle of the any BJT is to control the current of a third terminal with the voltage between the other two terminals. The principle of operation of NPNs and PNPs is exactly the same. The only difference is in their biasing and the polarity of the power supply for each type. ed

DESIGN NOTES

Low Power Op Amp: Low Power Filter, Headphone Driver Revisited

Design Note 563

by Aaron Schultz

Introduction

A new family of op amps features industry leading speed versus supply current. The LTC6261/LTC6262/LTC6263 family (single, dual, quad) provides 30MHz at a low 240µA supply current, with 400µV maximum offset voltage and rail-to-rail input and output. In combination with 1.8V to 5.25V supply, these op amps enable applications requiring uncompromised performance with low power and low voltage.

Bridge-Tied Differential Output Amplifier

The low supply current at the bandwidth and noise performance allows for excellent fidelity at a fraction of the usual dissipation in portable audio equipment. As with active filters, revisiting portable audio equipment headphone drivers is a rational enterprise, given the unique capabilities of the LTC6261.

Headphone speaker impedances range from 32Ω to 300Ω; their responsivity, from 80dB to 100dBSPL per 1mW and beyond. As an example, considering a headphone speaker with 90dBSPL per 1mW, it takes 100mW delivered to reach 110dBSPL. With 32Ω, the RMS current is 56mA and voltage 1.8V; with 120Ω, 29mA and 3.5V.

Given a 3.3V supply and the output of one LTC6261 amplifier, there may not be sufficient drive capability to yield 100mW. However, the combination of two 180° phased amplifiers is enough to provide the necessary drive to reach upwards of 100mW delivered power. Duplication of this bridge drive circuit enables power to both left and right sides.

The LTC6263 provides four amplifiers in one small package. Data from a 2-amplifier LTC6262 driving what could be left or right is shown in Figures 2 and 3. Basic current consumption of the two amplifiers, with as much as $1V_{P-P}$ input but no load, is 500µA.

The circuit consists of first, an inverting gain stage with closed loop gain = 1.5, and a subsequent inverting stage. The combination of inverting stages produces a single-ended input to differential output gain of 3.

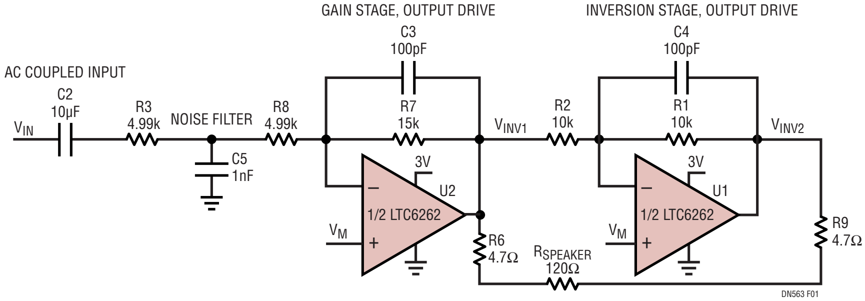


Figure 1. Audio Headphones Bridge Driver

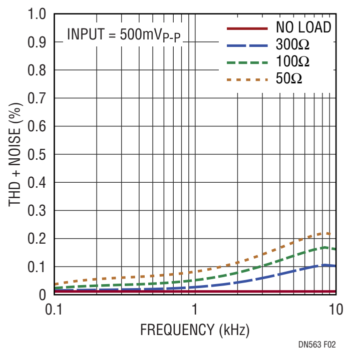


Figure 2. LTC6262 Bridge Driver THD and Noise with Different Loads vs Frequency

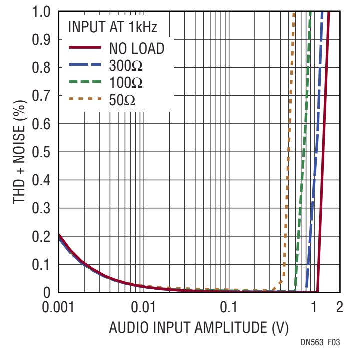


Figure 3. LTC6262 Bridge Driver THD and Noise with Different Loads vs Amplitude at 1kHz

With $500mV_{P\text{-}P}$ input, the output is $1.5V_{P\text{-}P}$, or 0.75V max, or $0.53V_{RMS}$. With 50Ω, 500mV input leads to approximately 5.6mW delivered power. At $1V_{P\text{-}P}$ input, the circuit delivers 22.5mW. Note that it helps that the LTC6261 output can swing close to rail-to-rail with load.

The first build of this circuit in the lab produced a significant tone at a few hundred Hz. It turned out that the positive input was not well grounded as an "AC ground" over all frequencies because the voltage was not strongly pegged. The need to peg the voltage arises when using a single supply rather than a dual supply. With a single supply, V_M is not ground, but rather a mid-rail voltage created to enable inverting topologies to work properly. The resistor divider that creates V_M has large resistance values (for example, two 470k in series) to minimize additional supply current. A large capacitor ensures a strong ground at low frequencies. Indeed, the addition of a large capacitor (1µF, which forms a pole with the 470k resistors in parallel) eliminated the mysterious distortion tone.

Despite the low quiescent current, this driver delivers low distortion to a headphone load. At high enough amplitude, distortion increases dramatically as the op amp output clips. Clipping occurs sooner with more loading as the output transistors start to run out of current gain.

One significant concern in a portable device is battery drain. Music played loudly, or listeners' musical choices affect the rate of battery drain. The end-use of a device is out of the designer's control. Quiescent current, though, is not. Because much of a device's time may be spent idle, quiescent current is significant, as it drains batteries continuously. The LTC6261's low quiescent current increases battery discharge time.

Conclusion

The applications shown here take advantage of a unique combination of features available in the LTC6261 op amp family. The low quiescent current of these devices does not diminish their ability to perform at levels usually reserved for more power hungry parts. Rail-to-rail input and output, shutdown, and choice of package are features that add to their versatility.

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WILLIAM WONG | Technology Editor

What's the Difference Between Machine Learning Techniques?

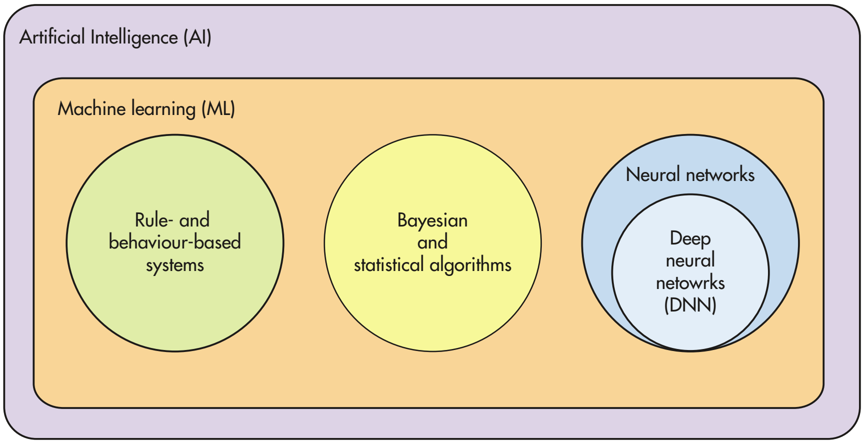
Machine learning is a hot topic, but what does this subset of artificial intelligence really mean?

Artificial intelligence (AI), machine learning (ML), and robots are the sights and sounds of science fiction books and movies. Isaac Asimov's Three Laws of Robotics, first introduced in the 1942 short story "Runaround," became the backbone for his novel *I, Robot* and its film adaptation *(Fig. 1)*. Although we are still far away from achieving what movie producers and sci-fi writers have envisioned, the state of AI and ML has progressed significantly. AI software has also been in use for decades but advances in ML, including the use of deep neural networks (DNNs), are making headlines in application areas like self-driving cars.

AI and ML research has been around since before computers even existed. Of course, they made practical creation and applications possible. The challenge has always been trying to keep up with the hype. Usually the programmers were unable to do so—hence, the many "failures" of AI.

In practical terms, AI essentially went underground, providing everything from expert systems to behavior-based vacuum cleaning robots like iRobot's Roomba. The latter used an 8-bit microprocessor running a behavior-based rule system. Likewise, e-mail spam filters have been using Bayesian statistical techniques for decades, with varying levels of success.

1. The movie *I, Robot* has robots that should be following Asimov's Three Laws of Robotics.



2. Artificial intelligence is a very large area of research of which machine learning is only one part. Three of the major areas of machine learning are shown here, but there are literally dozens that can be grouped in various ways.

AI is a very large area of research of which machine learning is only one part *(Fig. 2)*. The three examined here will be rule-based systems, Bayesian and statistical algorithms, and neural networks. These are presented in more detail later. There are more machine learning approaches not included in this list.

LEARNING STYLES

In addition to machine learning algorithms, there is the style of machine learning that can be employed. Some algorithms are more amenable to certain styles that include:

- Supervised learning
- Unsupervised learning
- Semi-supervised learning

Supervised learning has labeled training data, such as an e-mail that has been marked as spam. The training process usually generates improved accuracy over time. It is used in algorithms like back propagated neural networks.

Unsupervised learning does not have labeled data, and the result of the training is often unknown. This approach can be used for creating general rules.

Semi-supervised learning includes a mixture of labeled and unlabeled data. This approach is often used when the structure of the data needs to be understood and categorized in addition to allowing predictions to be made.

RULE-BASED AND DECISION TREE SYSTEMS

Rule-based and decision tree algorithms are the easiest to understand. Rule-based systems consist of a collection of logical rules or conditions based on inputs. A rule is triggered when its conditions are met. The triggered rules may change internal state variables, as well as invoke actions.

For example, a robot may have a number of sensor inputs that detect obstacles by touch, as well as inputs about its movement. A rule might cause the robot to stop if it is moving and an obstacle sensor is triggered.

Rules can generate conflicting actions in which case some priority mechanism needs to be implemented. For example, one rule action may stop a robot, while another wants to change its direction.

A rule- or behavior-based system normally moves from one state to the next, applying all the rules to each state. Not all rules need to be examined depending upon the implementation. For example, rules may be grouped by inputs, and some only need to be examined if an input changes.

Decision trees are a structure rule-based system where each node in a tree has conditions that allow classification by refinement as an algorithm traverses the tree. There are many popular algorithms in this space, including Classification and Regression Tree (CART) and Chi-squared Automatic Interaction Detection (CHAID).

One advantage of these approaches is the ability to backtrack the logic process used to perform an action or reach a conclusion. This is very valuable for debugging, but it can also be useful in the learning process. There is also the possibility of examining rules for proofs.

Finally, a simplistic presentation of a rule-based system where condition A and B invoke action C overlooks the possibility, and often requirement, that the logic involved is binary in nature. Probability can be used in a rule system, as well.

BAYESIAN AND STATISTICS

Bayes' theorem describes the probability of a test result based on prior knowledge of conditions that might be related to the result. The theorem relates the chance that an event A happened given the indicator X, Pr(A|X), to the probability of event X given A, Pr(X|A). It allows for correction of measurement errors if the real probabilities are known. Of course, test results come with test probabilities.

There are a number of Bayesian algorithms based on the theorem, including Naive Byes and Bayesian Belief Network (BBN). Like differential equations, the theory can be hard to understand, but the application is usually straightforward. As noted earlier, Bayes algorithms have been utilized in applications like e-mail spam filtering, but they are not limited to this narrow application.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Bayes is only one method that employs probability and statistics. There are also regression algorithms that have been used in machine learning. Popular regression algorithms include Ordinary Least Squares Regression (OLSR), Multivariate Adaptive Regression Splines (MARS), and, of course, linear regression.

There are also variants on regression that are used in machine learning, such as ridge regression. It is also known as weight decay. It is also known as the Tikhonov-Miller method and the Phillips-Twomey method. The variants look to simplify the models to reduce system complexity that provide better generalization support.

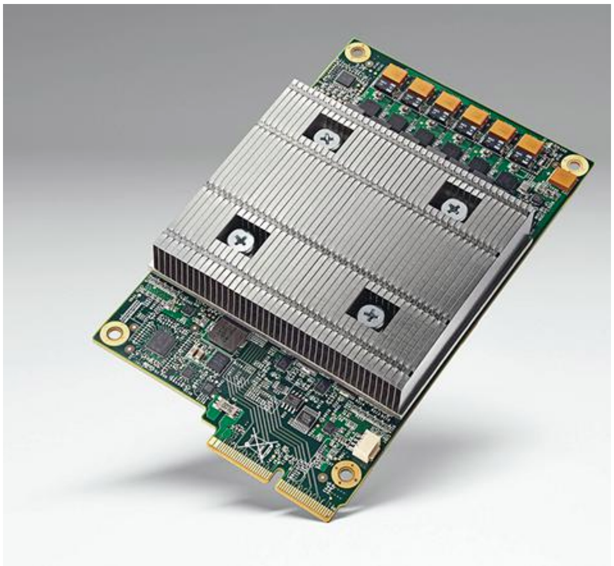
NEURAL NETWORKS

Artificial neural networks (ANNs) have been around for a long time, but their high computational requirements for complex networks has limited the use and experimentation until recently with multicore systems such as GPGPUs providing an economical platform for a variant called deep neural networks (DNNs).

Initially neural networks were of interest as a way of copying biological neural networks like the human brain. The brain is made up of neurons that are connected via an axon to synapse and dendrites on other neurons. The electrical signals from incoming signals are summed by the neuron. A result that exceeds a threshold sends a signal via the axon.

ANNs are built in a similar fashion, but using electronics or software. It takes many neurons to perform useful functions; the human brain has 100 billion. The trick to having something useful is the way the neurons are connected as well, as the weights associated with the neurons.

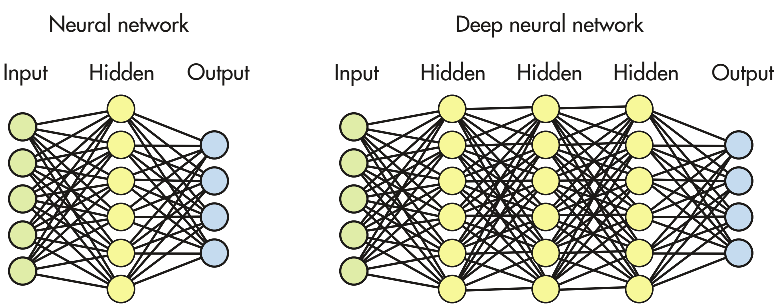
A basic neural network consists of a set of inputs and outputs with a hidden layer in between *(Fig. 3)*. A DNN has multiple hidden layers. The networks may be the same logically, but the number of inputs, outputs, and hidden layers varies as well as other configuration options. Of course, the key to a system's operation is the weights associated with the connections and nodes.



4. Google's Tensor Processing Unit (TPU) has a large, 8-bit matrix multiply system designed to accelerate DNN operations.

Neural networks require training to generate the weights used in the system. Systems can learn dynamically, but these tend to be more complex as training normally requires more computational horsepower than inference. Training uses a feedback system where an input is matched with outputs and the internal hidden layer weights are adjusted. This process requires more than just a few samples. A system with a large number of inputs like a photo image and a large number of sample sizes will often require a cluster or high end CPU and GPU to create a DNN configuration. On the flip side, a microcontroller may often be sufficient for some applications to utilize a DNN configuration to perform inferences in real time.

FPGAs and specially designed hardware to address neural networks are also available. There is even a hardware-based network on Intel's compact 32-bit, Quark-based Curie system-on-chip *(see "What Is Inside an IoT Chip?" on electronicdesign.com)*. The advantages of this approach are lower power requirements and higher performance operation.



3. A neural network consists of a set of inputs and outputs with a hidden layer in between. A deep neural network has multiple hidden layers.

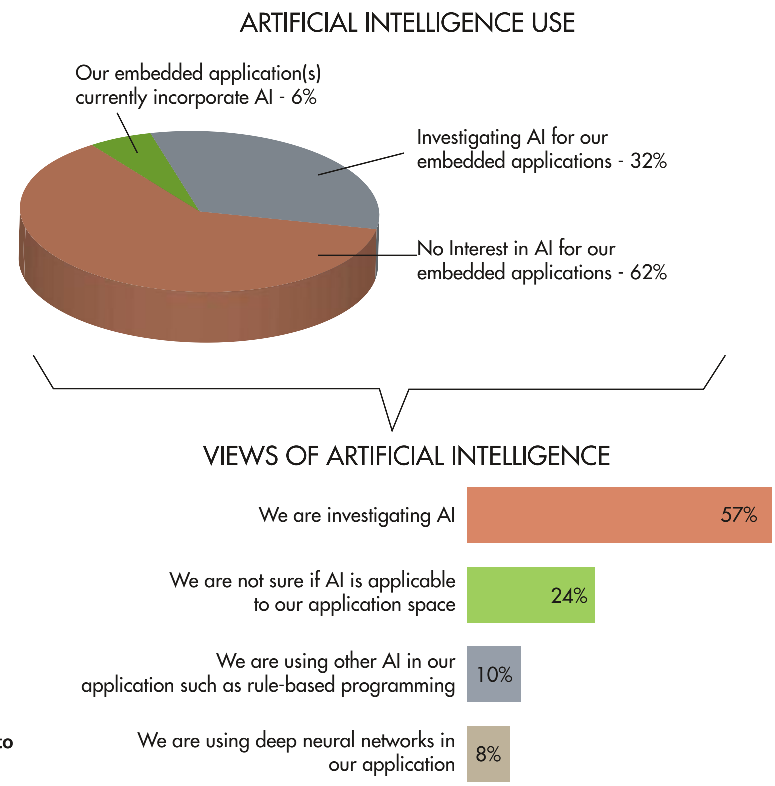
Google's Tensor Processing Unit (TPU) is designed to crunch 8-bit matrices that are common in DNN computations *(Fig. 4)*. Unlike number-crunching applications that require double precision floating point, DNN typically has weights that easily fit into 8-bits. The number of nodes tends to be more important than weight precision. The TPU will normally be used for training,

but it could be used in the cloud for running lots of inferences.

DNNs have been used for a wide range of applications, from identifying items in an image to voice recognition. These can be done with conventional DNNs, but there are other configurations that provide additional functionality. One of these configurations is convolutional neural networks (CNN).

Convolutional neural networks are feed forward ANNs that may constrain the nodes in three dimensions. CNNs consist of a stack of layers that include a convolutional, a pooling, and a fully-connected layer.

The actual design and configuration of neural networks is a bit more complex than presented here, although training and using the results on an existing system are much simpler. This typically entails providing training input and then deploying the results where a system might be used to identify dogs in photos.



5. More than half of the developers surveyed are looking into artificial intelligence, especially deep neural networks.

Deep neural networks (DNNs) have been used for a wide range of applications, from identifying items in an image to voice recognition. These can be done with conventional DNNs, but there are other configurations that provide additional functionality. One of these configurations are convolutional neural networks (CNNs).

Part of the challenge of using neural networks is that they are essentially black boxes. This can be an advantage, but it essentially hides what is going on inside the system. Properly preprocessing input can also be critical to the success of using neural networks. Likewise, neural networks are not applicable to every application, but they do work very well for many applications.

Finally, it is possible to have a neural network provide feedback on part of the reasoning behind their results, but in general they do not provide this information. That may not be a problem if the accuracy of the inference is sufficient for the application, like being able to identify a dog within a picture at least 95% of the time. On the other hand, a financial advisor might want to know what the credit risk model looks like for recommendations coming out of a neural network.

Neural networks are making many applications practical and there are a lot of platforms, hardware, and software being brought into play *(see "A Deeper Look at Deep-Learning Frameworks" on electronicdesign.com)*. *Electronic Design's* recent Embedded Revolution survey and white paper highlighted the number of embedded developers interested in AI *(Fig. 5)*.

AI and ML have been used productively for decades, even though AI has been criticized for the hype associated with the technology. DNNs and CNNs are currently being hyped, but they too are delivering on the promise. The trick is to understand that there are many techniques that can be used for a particular application, and to do more research to find out which will work best. ed ideas for design

Microcontroller Battery Monitor Circuit Needs Only One Pin

By TOMMASO ANGELINO | Sistemi Elettronici Angelino (S.E.A.), Italy

THIS CIRCUIT SOLVED a problem encountered in developing a portable device with an ARM Cortex-M0 processor. The power supply consisted of two AA batteries (2 × 1.5 V), and I needed to signal the user about the battery's state. The Cortex-M0 operates from 3.3 V down to 2.0 V, and an AA battery is considered discharged when its voltage drops to 1.1 V, so the available supply is 1.1 V × 2 = 2.2 V. This was a very low-power application that could work down to 2.2 V, so it was not necessary to warn the user to change the batteries until that voltage level was reached.

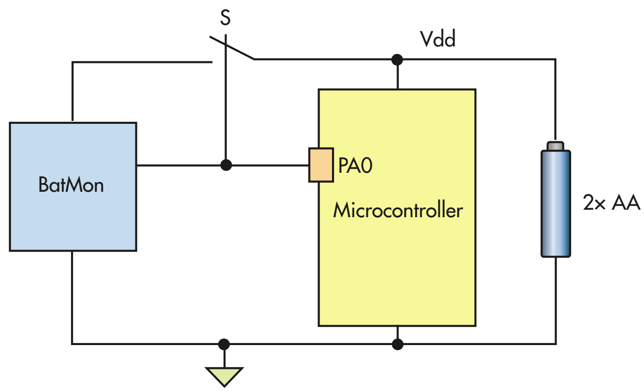
The microcontroller appears to offer a simple way to measure the battery voltage via its analog-to-digital converter (ADC). However, this did not seem to be a possible solution here, as the Cortex-M0 datasheet says the ADC will only work if its V_{DDA} is greater than 2.4 V (the ARM core operates from 3.3 V down to 2.0 V, but not all of its functions do). Tests showed good results only when V_{DDA} was at least 2.65 V. The obvious solution was to switch to another microcontroller such as a lower-power version, but this would mean rewriting and retesting the code, redoing of the printed-circuit-board layout, and ultimately increase cost in a volume application.

Instead, this circuit was developed to indicate the state of the batteries, using some standard discrete components. The battery monitor needed to:

- Use only one pin of microcontroller (important when using low pin-count device).
- Have very low current drain when in Idle state.
- Use the same pin to switch from Active to Idle state and to read the state.

Figure 1 shows how only one pin—PA0—of the microcontroller is used to implement the different functions for the battery-monitor (BattMon) circuit, driving switch S from Idle to Active mode, reading the state of the battery provided from BattMon, and going back from Active state to Idle state.

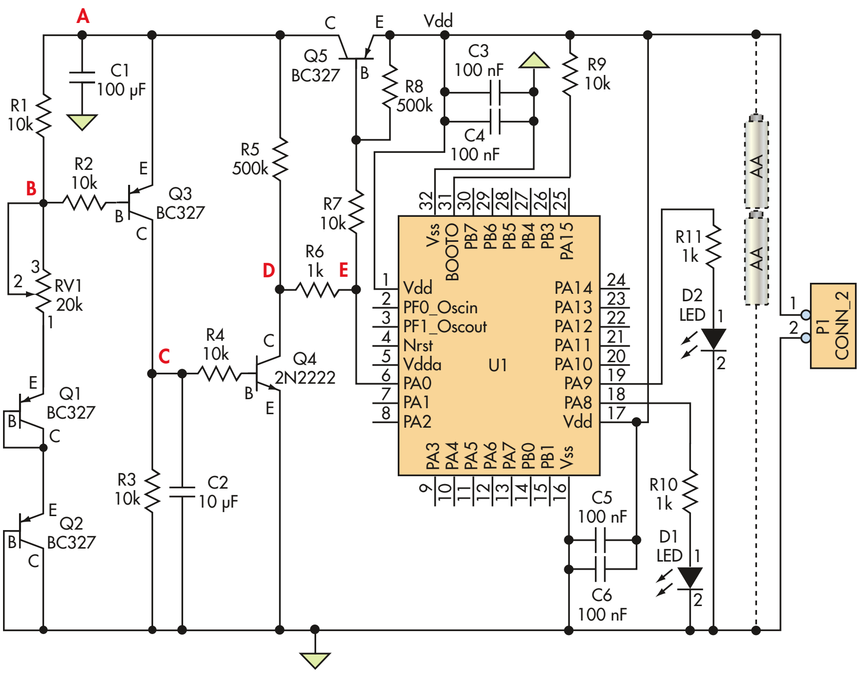
The complete circuit *(Fig. 2)* is powered by two AA batteries. Every n seconds (or even hours), the microcontroller decides to see if the battery level is over or under 2.2 V. When the microcontroller is not looking to check the battery voltage, it sets PA0 to high level, so Q5 is off. This assures that the current of the BattMon circuit *(the blue box of Fig. 1)* is very low, which is very important for a portable device. Measured current in this state is approximately 4 µA.



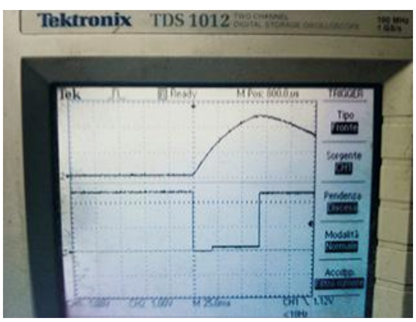
1. The basic concept of the battery monitor shows the relationship among functions and that only one pin of the microcontroller is used to implement the circuit.

When the microcontroller decides it needs to know the battery voltage, it sets PA0 low for 20 ms and switches Q5 on; this is the time needed to charge the capacitor C1 to $V_{DD} - V_{CESAT}$(Q5). After the 20 ms period, the microcontroller changes the state of PA0 from "out" to "in" mode, which sets Q5 to off, and for some period (depending on C-R values), the V_{DD} level is held by C1.

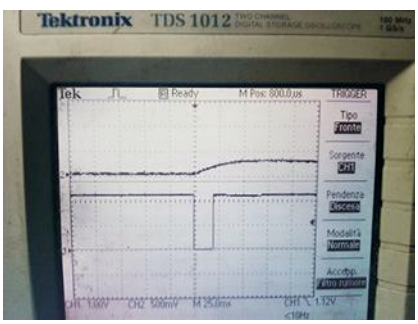
If V_{DD} is greater than 2.2 V, then V_{EB}(Q3) is above 0.7 V and Q3 is on; this condition depends on Rv1, Q1, and Q2, which are connected in diode mode and set the voltage at point B. By varying Rv1, we can vary the voltage value at point B and thus the voltage at point A, which changes Q3 from off to on and back. For this test, Rv1 was set to 12 kΩ. Then, with $V_{DD} \geq 2.2$ V, Q3 is on and the voltage at point C goes high, while Q4—which is needed to avoid R3/C2 pulling down point E point when it goes high from 0 to 20 ms—inverts it and produces a low voltage at point E. Thus, if $V_{DD} \geq 2.2$V, input PA0 will read a low value.



2. The detailed circuit uses five standard transistors plus passive components to implement the one-pin battery-monitor solution.



3. The bottom trace shows the microcontroller sampling the value at PA0 input after a 50-ms time delay from the start of the cycle (Ch 1: 25 ms/div horizontal, 1 V/div vertical).



4. The bottom scope trace shows the microcontroller sampling the PA0 input 50 ms from start of procedure (Ch 1: 25 ms/div horizontal, 1 V/div vertical).

The microcontroller will sample the value at PA0 input 50 ms from the start of procedure (t0 = 0), so it sets PA0 low at time t0 = 0, then sets PA0 to input mode after 20 msc. After 50 ms (from t0 = 0), it samples the value as seen in the bottom trace of *Figure 3*. The procedure ends with PA0 set to OUT mode and to a high level, which turns Q5 off and reduces the current draw of the BattMon section.

Next, follow what happens if V_{DD} is less than 2.2 V. As before, the sequence starts by setting PA0 low for 20 ms; this switches Q5 to on and charges C1. Next, it changes PA0 from OUT to IN mode, which switches Q5 off and lets C1 hold

V_{DD} for some time. But now $V_{DD} < 2.2$ V, so Q3 stays off because V_{EB}(Q3) < 0.7 V, while the voltage at point C stays low and points D and E go high. Therefore, if $V_{DD} < 2.2$ V, input PA0 will read a high value. Remember, the microcontroller will sample the value at the PA0 input 50 ms from start of procedure as shown in the bottom trace of *Figure 4*.

Note that the values of R1, R2, R3, R4, and R7 in the circuit are not optimized for performance; they have been optimized for production. It's possible to accelerate performance by adjusting the time scale by using 5 ms instead of 20 ms to charge C1, and sampling after 2 to 4 ms. Consequently, this will reduce the current required in active state, which is important if it's desired to check the state of the batteries more frequently.

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This code segment can be used to test the circuit:

```
Init(GPIO,Clock, etc..);
void Test_BattMon(void)
{
        // Using  pin PA0 to drive and to sample the Battery monitor
        while(1)
        {
                SetPA0Mode("OUT");          //Set PA0 = OUT
                ClrPA0;                     //Set Pa0= Low
                Delay(20);                  //Time to C1 to charge
                SetPA0Mode("IN");           //Set PA0 = IN
                Delay(30);                  //Delay to sample at 50ms
                if(ReadPA0==High)           //Battery Voltage under 2.2V
                        LedR_ON;            //Red Led On
                else                        // Battery Voltage over 2.2V
                        LedG_ON;            //Led Green On
                SetPA0Mode("OUT");          //Set PA0 = OUT
                SetPA0;                     //Set PA0 = High

                Delay(1000);
                LedR_OF;LedG_OF;
        }
}
```

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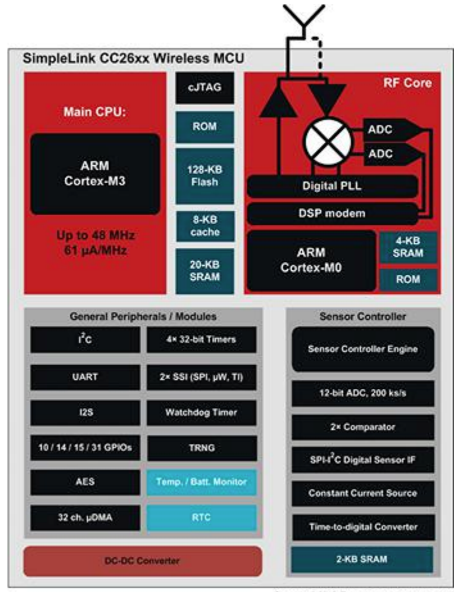
New Products

Wireless MCUs Add Memory / Bluetooth 5 / Automotive

TEXAS INSTRUMENTS is offering two new devices in its scalable SimpleLink BLE wireless MCU family adding more available memory, Bluetooth 5-ready hardware, automotive qualification and a new ultra-small WCSP option. The CC264x devices feature a complete single-chip hardware and unified software solution with an ARM Cortex-M3 based MCU, automatic power management, full-featured Bluetooth-compliant radio and low-power sensor controller.



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The Bluetooth 5-ready SimpleLink CC2640R2F wireless MCU offers more available memory and comes in a 2.7 x 2.7 mm WCSP option, delivering the longest range with the lowest power consumption. The CC2640R2F-Q1, offered in a wettable flank QFN package, enables smartphone connectivity for car access including PEPS and RKE, as well as automotive uses with AEC-Q100 qualification and Grade 2 temperature rating. For applications such as car access, assisted parking, car sharing and in-car cable replacement, the Q1 device will support Bluetooth 5 in the second half of 2017.

The CC2640R2F wireless MCU LaunchPad development kit LAUNCHXL-CC2640R2 is available for $29. The CC2640R2F wireless MCU is available now for mass production in 2.7 x 2.7 mm WCSP and 4 x 4, 5 x 5 and 7 x 7 mm QFN packages starting at $2.00 each/1,000. The CC2640R2F-Q1 wireless MCU is available in a 7 x 7 mm QFN package starting at $6.99 each/1,000.

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Out-of-Box Tool Speeds Cloud-Based IoT Development

ENCOMPASSING BOTH hardware and software elements, ON Semiconductor's IoT Development Kit (IDK) utilizes a unique modular construction to present a configurable platform that enables the evaluation and development of highly differentiated IoT systems. The inherent flexibility of the IDK offers the necessary scope to address industry sectors such as environmental monitoring, healthcare, home/building automation, industrial control, and wearable electronics.

The IDK's baseboard features ON Semi's NCS36510 SoC, with a low power-optimized 32-bit ARM Cortex-M3 core, running the ARM mbed OS. By attaching different daughter boards to the Wi-Fi enabled baseboard, connectivity protocols enabled by ultra-low power radios, sensors, heart rate monitors, bio sensor interfaces and actuators can be added to the system. In addition, the portfolio includes support for numerous functions for implementing security, including encryption, secure debug, secure boot, and authentication.

An Eclipse-based IDE that includes a C++ compiler, debugger, and code editor. A comprehensive set of application examples, use cases, and related libraries have also been incorporated into the package. In addition to the default cloud software platform, support for industry standard Cloud connectivity protocols (MQTT and REST) is included.

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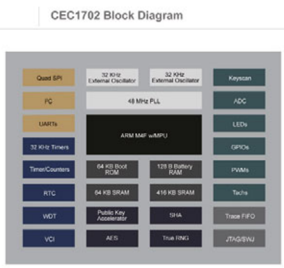

Full-Featured MCU Streamlines Security Implementation

THE CEC1702 cryptography-enabled MCU, now available from Microchip Technology, addresses the need for security measures, such as secure boot, driven by the growing expanse of IoT applications. The low-power but powerful, programmable 32-bit ARM Cortex-M4-based MCU offers encryption, authentication, private and public key capabilities and minimizes customer risk. It also provides performance improvements when compared to firmware-based solutions.

A hardware cryptographic cipher suite reduces compute time by orders of magnitude over software solutions, and, as an example, boasts a 20-50x performance improvement for PKE acceleration as well as 100x improvement for encryption/decryption. Whether it's being used as a security co-processor or a standalone MCU, the device offers a multi-dimensional defense against attacks, including: pre-boot authentication of system firmware; firmware update authentication; authentication of system critical commands; and protection of secrets with encryption.

A full development suite including hardware and software tools as well as peripheral libraries and crypto APIs help to speed up design cycles. The CEC1702Q-B1-SX hardware cryptography-enabled MCU is available in production volume for $2.60 each/10,000.

MICROCHIP TECHNOLOGY

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Fiber-Optically Isolated Probe Measures Floating Signals

THE HVFO103 from Teledyne LeCroy is a high-voltage fiber-optically isolated 60-MHz oscilloscope probe that is optimally designed for the measurement of small signals floating on a high voltage bus in power electronics designs. Optical isolation between the probe tip and the oscilloscope input reduces noise, distortion, ringing, overshoots, transients on the measured signal, and adverse loading of a device under test.

The 60 MHz fiber optic probe includes soft-carrying case, transmitter, receiver, 1m fiber optic cable, set of three micro-grippers, and a USB charging cable.

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DRIVERLESS CARS: Can We Regulate an Emerging Technology?

At a recent conference, Congressman Dan Lipinski talked about the benefits of self-driving cars and future regulations.

Dan Lipinski, a U.S. Representative for Illinois' 3rd congressional district and vocal voice for cybersecurity in transportation systems, delivered the keynote address at the recent The Empire State of Mobility Conference during the NY Auto Show. Lipinski, who serves on two House Committees—Transportation & Infrastructure, and Science, Space, & Technology—underscored the advantages of new mobility technologies during his presentation.

Much of the address focused on the benefits of driverless-car technology for our society and how new modes of mobility will transform the transportation system. He also emphasized the need for appropriate federal regulations, noting that they could safely speed up the rollout of this emerging technology.

Proponents of driverless-vehicle technology say that such vehicles will likely improve road safety, as most accidents result from human driver errors. They also point out that driverless cars have the potential to reduce traffic congestion while cutting pollution. These cars could even improve the mobility of the elderly and people with some kind of physical impairment.

GETTING MORE CONNECTED

To maximize the efficiency of driverless cars, Congressman Lipinski emphasized the importance of car connectivity. Car connectivity is expanding and at the same time changing the concept of mobility. New mobility behaviors like ride sharing are growing with companies like Uber, Lift, Car2Go, and Zipcar. With driverless cars, user behavior will change even more dramatically.

Rapid changes also are being seen in the automotive market, as technology advances bring sophisticated connectivity and safety features to a wider array of cars. Consequently, the driving experience will, in a not-too-distant future, reach a level where paying attention to the road or holding the steering wheel will not be required. For me personally, it's still hard to imagine that not knowing how to drive a car won't be an obstacle to "driving" that car.

The faster pace of the technology is evidenced by several U.S. companies announcing that they expect to debut fully automated (driverless) vehicles by the late 2020s (Ford is one example). But I don't think we will have "Level 5" *(Fig. 2)* driverless cars cruising the streets in the near future, because the technology is not yet on track. In addition, costs are still extremely high and regulations lack clarity at this point.

REGULATORY JUMBLE

Although many driverless car companies have tested their driverless cars on public roads, they're experiencing delays because of both technology challenges and regulatory issues. Just recently, Michigan became the first state to establish regulations for the testing, use, and eventual sale of self-driving cars. But should the state regulate the adoption of such a disruptive technology? Or should it be the federal government in order to avoid a state-to-state approach that could slow down technology development?

The U.S. Department of Transportation (DOT) recently released guidelines for autonomous vehicles, but it's still unknown how the DOT is going to implement them. For example, the DOT recommends that states be responsible for licensing human drivers, enforcing traffic laws, and establishing requirements for autonomous vehicle testing on public roads. For its part, the federal government should have primary control over the actual automation software and handling recalls.

I agree with Congressman Lipinski when he says that America needs better guidance from the federal government so as to not delay these advances. The U.S. should be a leader of the driverless car market by maintaining a balance between safety and innovation. Driverless-car technologies are disrupting multiple aspects of our society. As such, their rollout demands careful study and the participation of both the private and the public sector. ed

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Internal 30A/300μΩ Sense Resistor with 1.0% Current Accuracy

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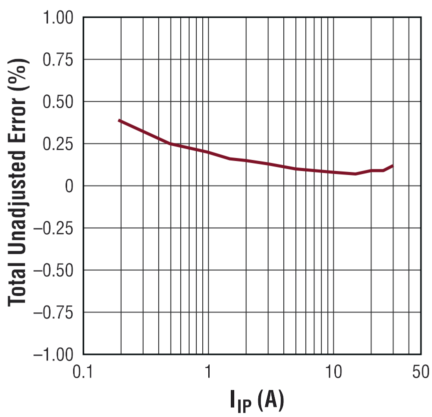
TUE Current Sense ADC vs Current



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